

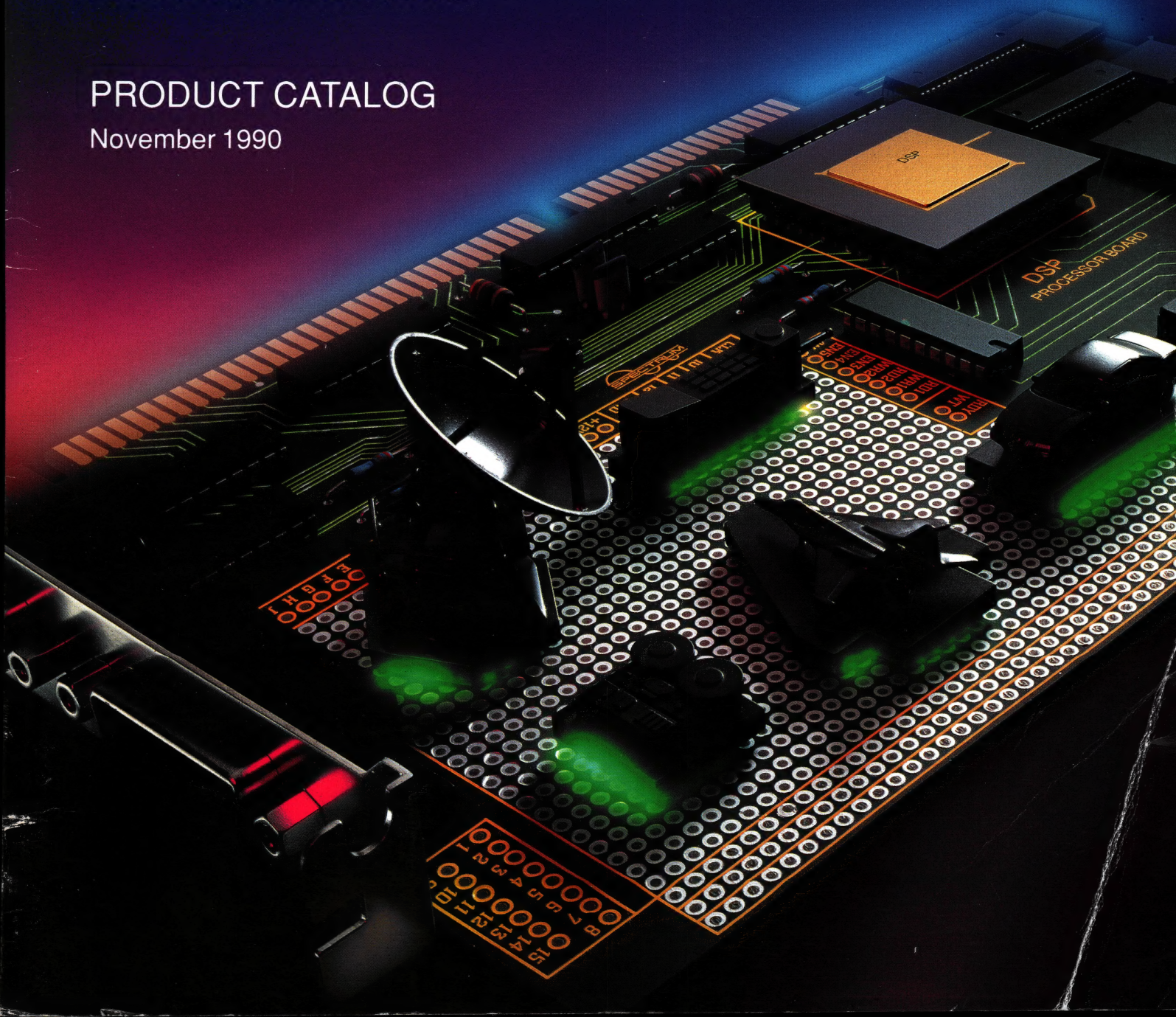


DIGITAL SIGNAL PROCESSING

*DEVELOPMENT TOOLS
AND OEM SOLUTIONS*

PRODUCT CATALOG

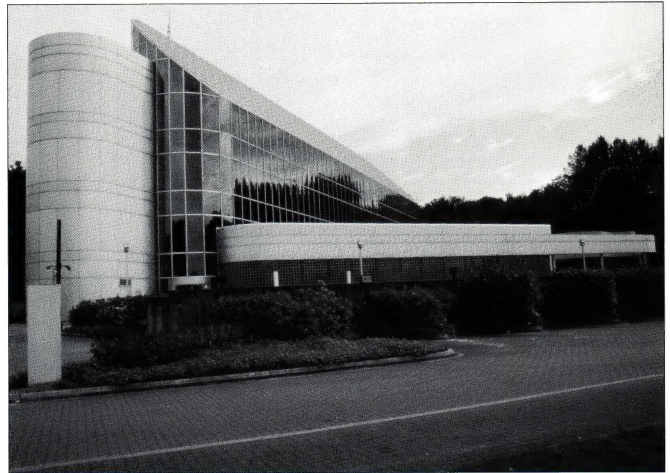
November 1990



Spectrum Signal Processing Inc.

Spectrum designs and manufactures specialized Digital Signal Processing computer hardware and software for the IBM PC/XT/AT and VME bus. The company provides its customers with leading-edge solutions to engineering challenges, enabling them to take advantage of this technology more quickly and economically than previously possible. Since its inception, Spectrum has introduced many unique products to the marketplace.

Spectrum's head office is located at Discovery Park in the Vancouver suburb of Burnaby, British Columbia. This facility houses marketing, engineering and administrative staff. Spectrum also maintains a sales office in Massachusetts.



ORDERING INFORMATION

The following information is intended to provide basic procedural instructions to SPECTRUM customers. If you want clarification or need help to deal with a situation not covered here, simply telephone the SPECTRUM office nearest you.

PLACING AN ORDER

When ordering SPECTRUM product, please provide the name and part number listed in this catalog. Orders may be placed by letter, FAX or telephone at the numbers shown below. All orders need a Purchase Order number, "ship-to" and "bill-to" addresses, method of shipment and a contact name. Since SPECTRUM usually ships orders upon receipt (inventory permitting) we do not provide Order Confirmation to the purchaser. Therefore, please specify upon ordering if you need an Order Confirmation. To order call:

Eastern US: 800-323-1842
Europe & UK: (508) 366-7355 (within Massachusetts)
FAX (508) 898-2772

Western US: 800-663-8986

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FAX (604) 438-3046

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All SPECTRUM products are packed and shipped with relevant documentation in rugged anti-static packaging to ensure safe delivery under normal shipping conditions. Please specify your preferred mode of shipment - be it 'Overnight', '2-Day Air' or 'Ground'. Unless otherwise instructed, all products are shipped via UPS 'Ground' with delivery charges prepaid by SPECTRUM and billed to you. Any brokerage fees arising from the shipping process are billed to the customer. SPECTRUM

makes every effort to meet special customer needs. If you require a "RUSH" shipment we do our best to meet your timing.

PRICES

All prices are in U.S. Dollars, F.O.B. Westborough, Massachusetts or Burnaby, B.C. Canada. Applicable Federal, State and Local taxes are extra. SPECTRUM reserves the right to amend pricing without notice.

TERMS

Net 30 days for accounts meeting established credit criteria, otherwise pre-payment is required.

QUOTATIONS & DISCOUNTS

SPECTRUM will provide a Letter of Quotation upon request, valid for 30 days unless otherwise specified. Volume discounts or OEM Cumulative Quantity Discounts are available on an order or contract basis.

ORDER CANCELLATION & 'RETURNS'

All orders placed with SPECTRUM Signal Processing are binding. Hardware items may be returned up to 30 days after receipt, and will be subject to a 15% restocking charge. If a hardware order is cancelled after product shipment it is considered a "Returned" item and is subject to the 15% restocking charge. When an item is being returned, a customer must obtain a Return Material Authorization (RMA) number and shipping instructions from Customer Service at 1-800-663-8986 (in USA) or (604)438-7266 (in Canada). SPECTRUM will not allow customers to return software purchases.

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Introduction to Spectrum

Spectrum's mission is to help first time users of DSP and experienced professionals build better products using DSP technology. We accomplish this by providing users with a total solution from proof of concept through to final production of DSP sub-systems.

Spectrum provides a combination of products that are unique to the DSP market. These include DSP development tools, applications consulting and standard off-the-shelf hardware products that are targetted for general purpose and many application-specific uses.

DSP development tools let customers test their new ideas without going through the expense of developing a system from scratch. Once the idea has been proven, the customer uses the same tools for detailed application programming and hardware prototyping.

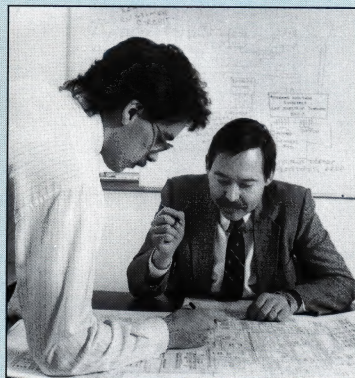
In many instances, customers will be working with DSP technology for the first time or they may encounter applications that require unique technical or project management skills. Spectrum's team of applications engineers provide applications consulting in both hardware and software design for a wide variety of application areas.

Development tools and applications consulting allow customers to quickly design Spectrum's systems into their products. Once the design is complete, these off-the-shelf systems provide customers with "fast to market" and cost effective solutions. Further cost reduction and additional functionality can be gained by customizing these standard products.

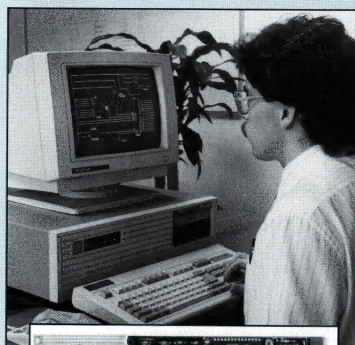
With our "EasyDSP" program, Spectrum has the capability to customize off-the-shelf products to meet customers' unique requirements.

"EasyDSP"

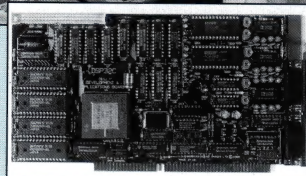
"EasyDSP" is a program targetted at first time users of DSP and experienced professionals requiring rapid development of DSP sub-systems. The process of taking a customer concept into a completed DSP sub-system involves several distinct stages:



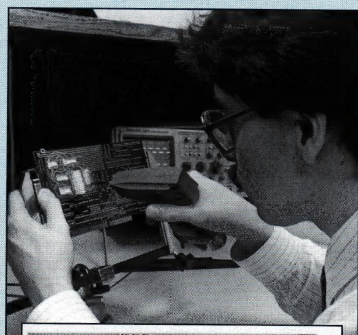
1. The customer and a Spectrum applications engineer develop a system specification. Spectrum engineers then design hardware to meet the customer's unique I/O requirements.



3. The resulting schematic is captured using in-house CAD tools to generate the final printed circuit layout for the sub-system.

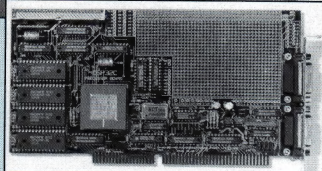


Completed DSP Sub-system



2. The design is bread-boarded using the prototyping area of Spectrum's new line of processor boards, the first being the DSP32C Processor Board.

Software is then debugged using Spectrum's development tools. Both the hardware prototype and software are tested to verify that the design meets specifications.



DSP32C Processor Board



4. The DSP sub-system is then integrated into the customer's system. Typically this system is based on an IBM-PC or compatible which is available in both desk top or rack mount

Product Overview

Introduction

Spectrum's line of standard products can be used as both development tools and end application systems. A variety of DSP engines are coupled with flexible analog and digital I/O to address customers' unique application requirements with an "off-the-shelf" solution. Development and application tools provide the software necessary to implement state-of-the-art DSP systems.

System and Processor Boards

Spectrum Processor Boards contain a DSP processor, expandable memory, serial I/O and DSP~LINK, our proprietary parallel interface. These boards provide all the resources necessary to implement DSP algorithms on digital data.

System Boards have the same basic resources as the Processor Boards and also include on-board analog I/O. Both System and Processor Boards can connect to DSP~LINK peripherals.

DSP~LINK Peripherals

DSP~LINK Peripherals are PC plug-in cards that provide additional off-the-shelf analog or digital interfaces. Spectrum is continually developing new peripheral boards to help users configure systems that match a wide variety of I/O needs.

Application-Specific Boards

A number of specialized boards are available for image processing, telecommunications, professional audio and data acquisition. In most cases, these products contain analog I/O which is designed for the specific application. Other interfaces can be added to the boards via DSP~LINK.

Software Development Tools

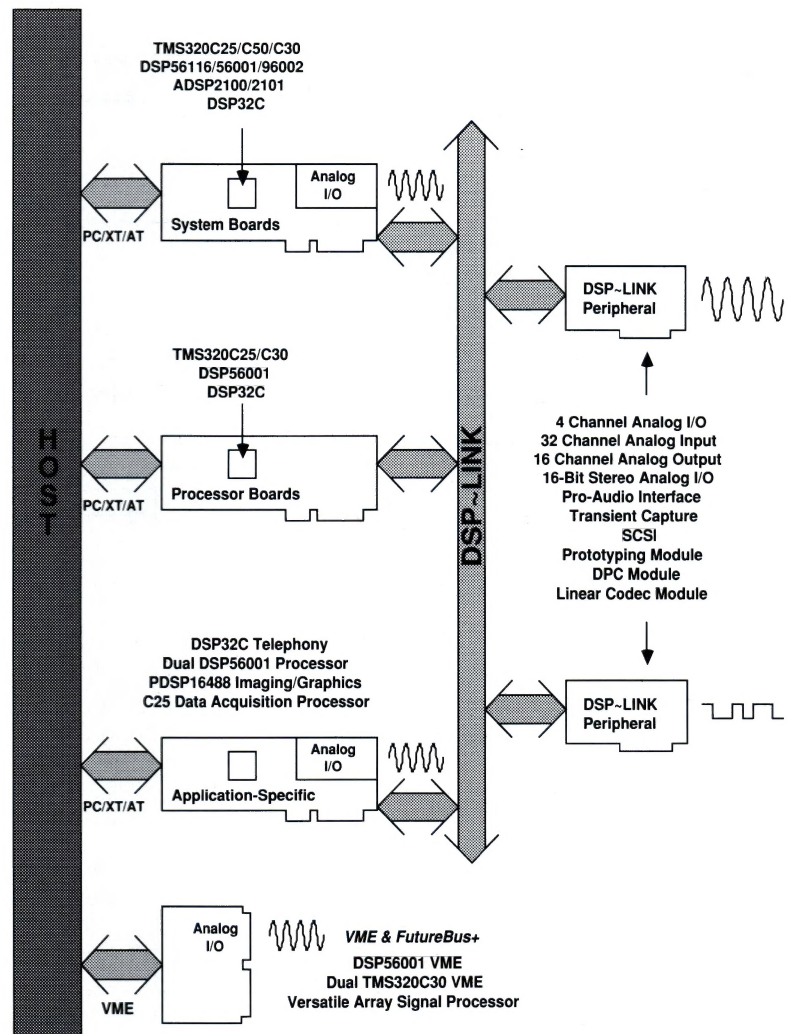
Spectrum offers software tools that address DSP chip code development, PC code development, data analysis and filter design.

DSP chip code development tools include Assemblers, Simulators, and 'C' Compilers, as well as debug monitors which are included with each board. High-level tools such as the SPOX™ applications programming interface provide a vehicle for quick custom program development.

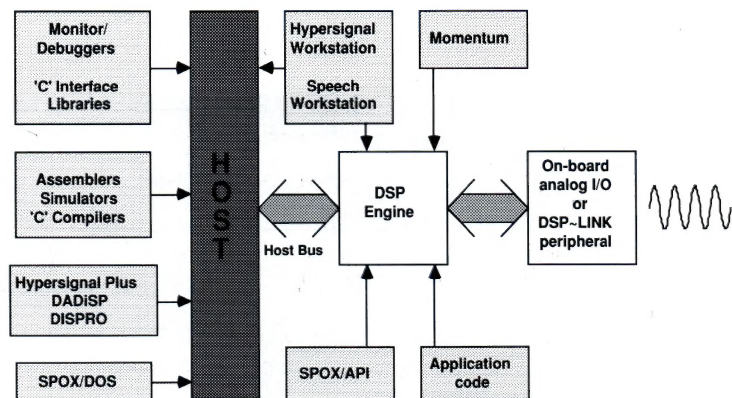
Software tools also include a High-Level Language Library of board interface functions (object loader, data transfer, initialization, and hardware control) complete with examples.

Data Analysis and Filter Design software includes standalone PC packages such as DADiSP and DISPRO, and packages that are integrated with certain Spectrum boards such as Hypersignal Workstation and Momentum Filter Design.

HARDWARE PRODUCTS

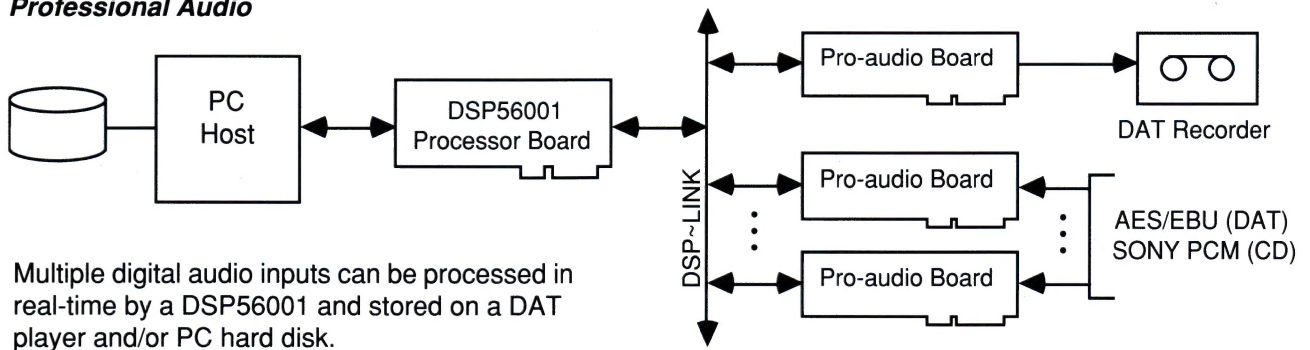


SOFTWARE PRODUCTS

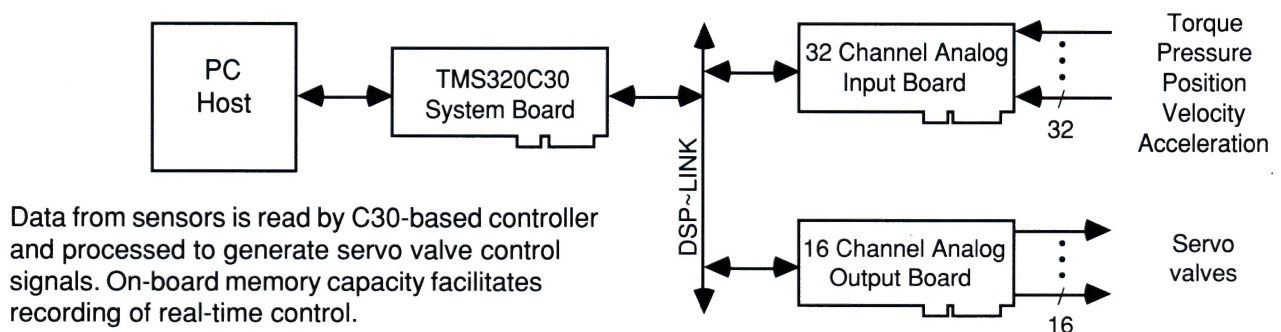


Typical Applications of Spectrum Products

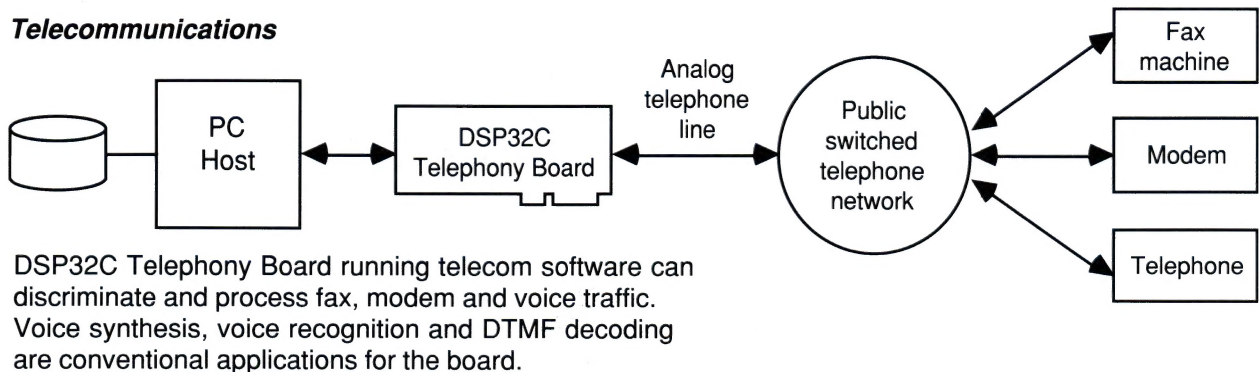
Professional Audio



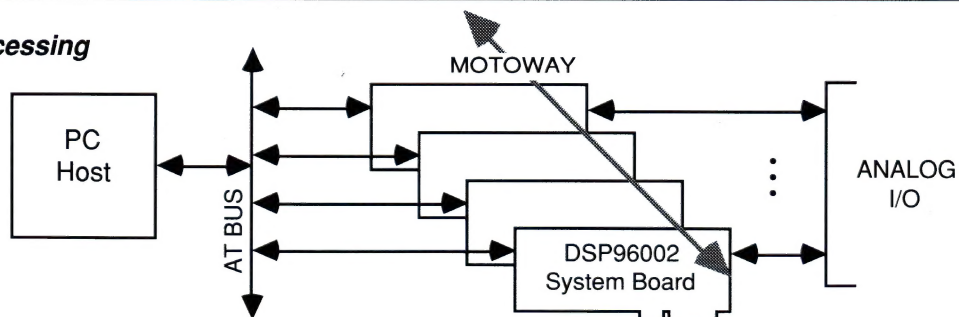
Multiple Input Multiple Output Feedback Control



Telecommunications



Array Processing



DSP~LINK System Expansion Interface

SPECTRUM's System and Processor Boards are equipped with the DSP~LINK system expansion interface. DSP~LINK is a bi-directional, 16-bit parallel bus that provides a high-bandwidth data path between the DSP device and peripheral expansion boards.

The System and Processor Boards are bus "masters" which directly control DSP~LINK Peripheral "slave" boards. Many off-the-shelf peripheral (slave) boards are available, enabling users to quickly configure their DSP system.

SPECTRUM encourages user-design of custom peripherals for this "open-architecture" bus. Custom interfaces can be quickly designed using the DSP~LINK Prototyping Module and Technical Application Notes.

FEATURES

- Separate from the IBM PC bus, avoids "PC Bottleneck".
- "Minimum Subset" of standard signals allows compatibility between all SPECTRUM master and slave boards.
- "Additional Signals" allows taking advantage of features found only on certain DSP chips.
- Open architecture allows users to design custom interfaces.
- Full specifications available in Technical Application Notes.

- Many off-the-shelf peripheral slave boards are available.
- Master-Slave connection via standard 50-conductor ribbon cable.

STANDARD SIGNALS AND ADDITIONAL SIGNALS

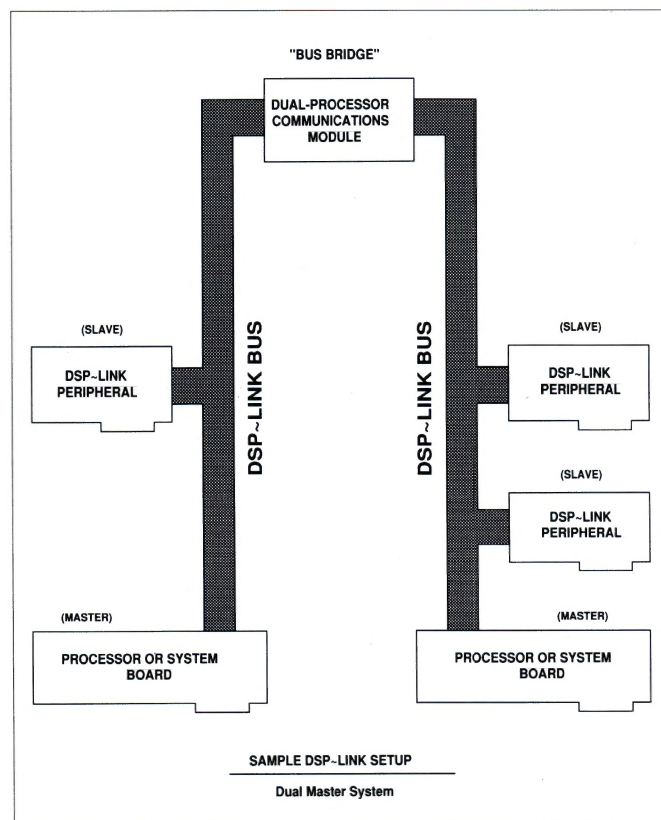
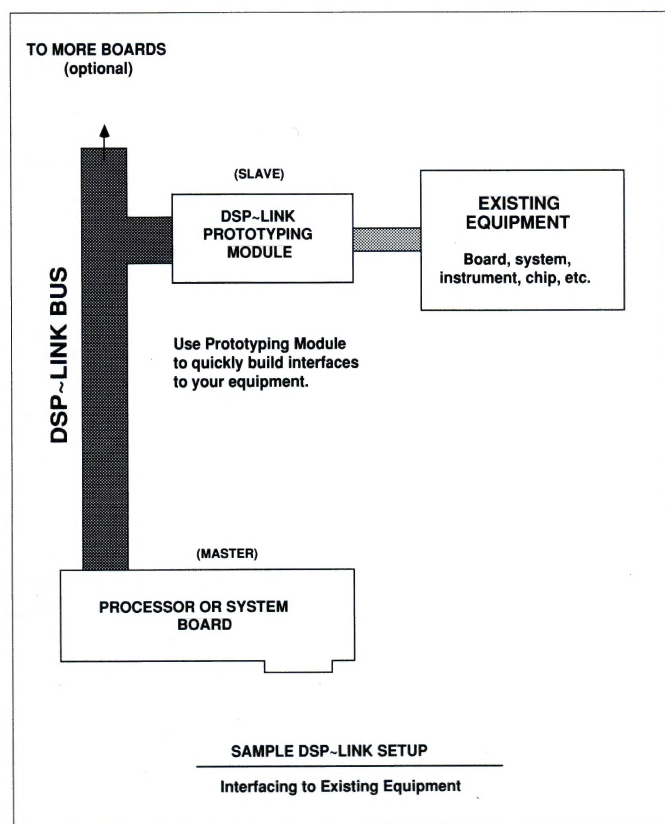
DSP~LINK is essentially a buffered extension of the DSP chip's local bus signals, and a subset of those signals are made to conform to a "minimum subset standard". This subset of signals is implemented on all boards that support DSP~LINK. This makes it possible to design DSP~LINK slave boards that will work with any DSP~LINK master board.

Since different DSP chips have different control signals, DSP~LINK allows using "additional signals" that are unique to a particular DSP chip.

DATA TRANSFER RATES

DSP~LINK supports 16-bit parallel transfers at a maximum rate of 5 Million 16-bit words/sec, including some software overhead. A more typical "Peak Software Transfer Rate" is approx 3 Million words/sec. The actual transfer rate depends on the particular master and slave boards being connected.

Refer to the "DSP~LINK Technical Application Note" for a more detailed analysis of DSP~LINK.



System Boards

Selection Guide

PRODUCT	TMS320C25 System Board	TMS320C50 System Board	TMS320C30 Real-Time Sys.	DSP56001 System Board	DSP56116 System Board	DSP96002 System Board
Part Number	600-00103	600-01056	600-00545	600-00202	600-01101	600-00993
Host Bus	IBM AT/XT	IBM AT/XT	IBM AT	IBM AT/XT	IBM AT	IBM AT
Processor Instruction Cycle Precision Accumulators Internal Memory	100ns ⁽¹⁾ 16-bit integer 1 x 32-bit 544 Words	50ns 16-bit integer 1 x 32-bit 9216 Words RAM 2048 Words ROM	60ns 32-bit floating pt. 8 x 40-bit 2048 Words 64 Word CACHE	100ns 24-bit integer 2 x 56-bit 1024 Words	25ns 16-bit integer 2 x 40-bit 4K Words	60ns 32-bit floating pt. 1 x 32-bit 1024 Words (PGM) 1024 Words (DATA)
On-Board Memory Standard Maximum	16K x 16 128K x 16	16K x 16 (PGM) 16K x 16 (DATA) 64K x 16 (PGM) 64K x 16 (DATA)	128K x 32 256K x 32	48K x 24 192K x 24	32K x 16 128K x 16	64K x 32 ⁽²⁾ 0 ws 256K x 32 ⁽²⁾ 1 ws 1088K x 32
Serial I/O	1 Synch (5 Mbps)	2 Synch (10 Mbps)	2 Synch (8.3 Mbps)	1 Synch (5 Mbps) 1 Asynch (2.5 Mbps)	2 Synch (20 Mbps)	None
Parallel I/O Interface	DSP~LINK	DSP~LINK	DSP~LINK	DSP~LINK	DSP~LINK	DSP~LINK
Analog I/O Channels Resolution Max. Sampling Rate	1 channel I/O 16-bit/12-bit 54 KHz/100 KHz	2 channel I/O 18-bit 200 KHz/ch	2 channel I/O 16-bit 153 KHz/ch	2 channel I/O 16-bit 153 KHz/ch	2 channel I/O 16-bit Delta Sigma 50 KHz/ch	2 channel I/O 16-bit Delta Sigma 100 KHz/ch
Application Software Real-Time O.S. C Compiler/Assem. Data Acquisition	None TI or LSI Hypersignal	None TI Hypersignal	SPOX™ TI Hypersignal	None Motorola Hypersignal	None Motorola None	SPOX™ Moto\Intermetrics Hypersignal

Footnotes:

(1) 80ns with TMS320C25-50 MHz

(2) Split equally between Port A and Port B

System Boards

Selection Guide

PRODUCT	ADSP-2100 System Board	ADSP-2101 System Board	DSP32C System Board	DSP32C Telephony Board	PDSP16488 Imaging/ Graphics Brd.
Part Number	600-00167	600-00671	600-00455	600-00851	600-00879
Host Bus	IBM AT/XT	IBM AT/XT	IBM AT ⁽³⁾	IBM AT ⁽³⁾	IBM AT/XT
Processor					
Instruction Cycle	100ns	80ns	80ns	80ns	8-bit
Precision	16/24-bit integer	16/24-bit integer	32-bit floating pt.	32-bit floating pt.	microprocessor
Accumulators	1 x 40-bit	1 x 40-bit	4 x 40-bit	4 x 40-bit	supervising
Internal Memory	16x24-bit CACHE	2K x 24-bit 1K x 16-bit	1536 Words	1536 Words	8 x 8 2D Convolver
On-Board Memory					
Standard	8K x 24 (PGM) 8K x 16 (DATA)	4K x 24 (PGM) 4K x 16 (DATA)	40K x 32	40K x 32	256K Byte
Maximum	32K x 24 8K x 16	14K x 24 12K x 16	136K x 32	136K x 32	256K Byte
Serial I/O	None	2 Synch ⁽⁴⁾ (6.25 Mbps)	1 Synch (16 Mbps)	None	None
Parallel I/O Interface	DSP~LINK	DSP~LINK	DSP~LINK	DSP~LINK	None
Analog I/O					
Channels	1 channel I/O	2 channel I/O	2 channel I/O	1 channel I/O	2 in ⁽⁵⁾ / RGB out
Resolution	12-bit	14-bit codec	16-bit	linear codec	8-bit
Max. Sampling Rate	125 KHz	19.2 KHz	153 KHz/Ch		10 MHz
Application Software					
Real-Time O.S.	None	None	None	None	None
C Compiler/Assem.	Analog Devices	Analog Devices	AT&T	AT&T	None
Data Acquisition	Hypersignal	Hypersignal	Hypersignal	None	None

Footnotes:

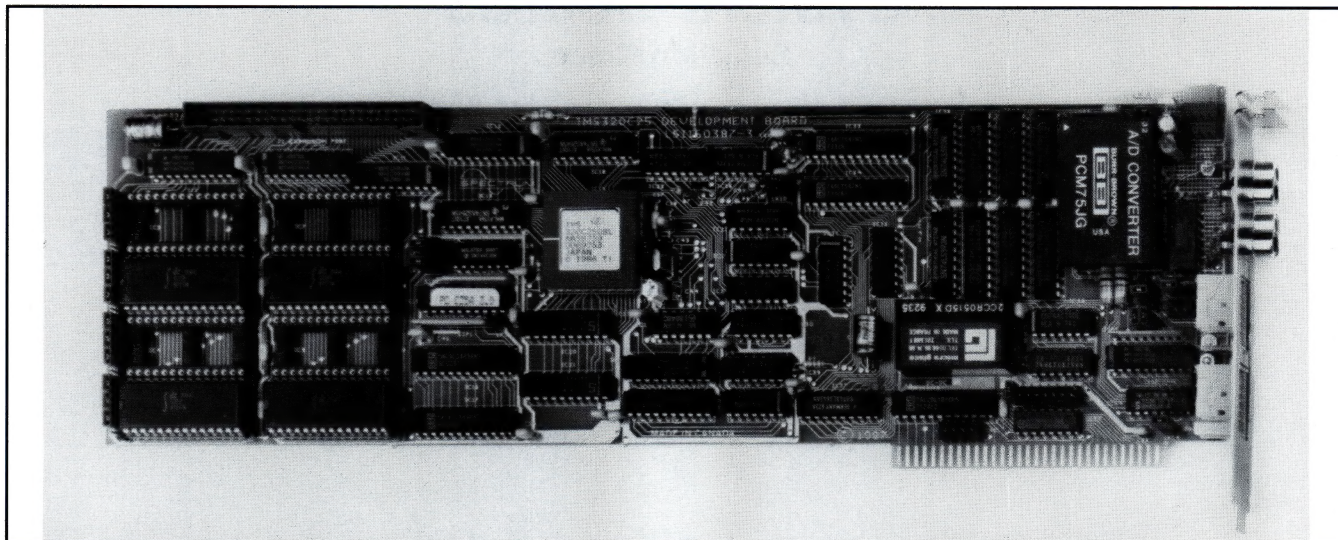
(3) Full DMA implementation

(4) 12.5 Mbs if external clock is used, available only when analog I/O not in use

(5) Multiplexed video inputs

TMS320C25 System Board with Development Support

Part Number: 600-00103



FEATURES

- TMS320C25 16-bit 100 ns processor.
- **DSP~LINK** System Expansion Interface.
- 128 Kwords of on-board memory capacity.
- High speed 16-bit A/D and D/A with sample-and-hold.
- Global memory capability via DSP~LINK.
- 5 Mbps full-duplex serial I/O.
- IBM PC/XT/AT or true compatible plug-in board.
- Complete debug monitor.
- 'C' board drivers.

The system runs at full speed (100ns instruction cycle) and comes with 16 Kwords of 35ns static RAM for zero wait-state operation.

Occupying only 8 I/O locations in the PC's address space (relocatable to 8 places), users may configure up to 8 boards in one PC. There are on-board address counters for efficient block transfer operations. The PC has direct access to all external RAM, and can read and write programs while the processor is running.

In addition to on-board analog interfaces, data can also be acquired via the **DSP~LINK** system expansion interface. This 50-pin standardized expansion bus is featured on most SPECTRUM products including multi-channel data acquisition cards, providing users with the flexibility of tailoring a system to match their analog I/O requirements.

SPECTRUM provides a similar board without analog I/O called the "TMS320C25 Processor Board". Please refer to the appropriate data sheet for information on this product.

DEVELOPMENT SUPPORT

A complete debug monitor is provided for software development and debugging. Monitor features include single-step,

breakpoint, disassembly, program loading, data upload/download, register inspection/modification, and full speed operation.

Sample programs familiarize the user with program development and give good examples of how the system can be used in the PC environment. These sample programs include a 128 point FFT, a real-time FIR filter, and a data logger. Source code for these programs is included as part of the system documentation.

A library of 'C'- callable board drivers for the PC is provided including 'C' and assembly source code, Microsoft linkable object modules, and many examples.

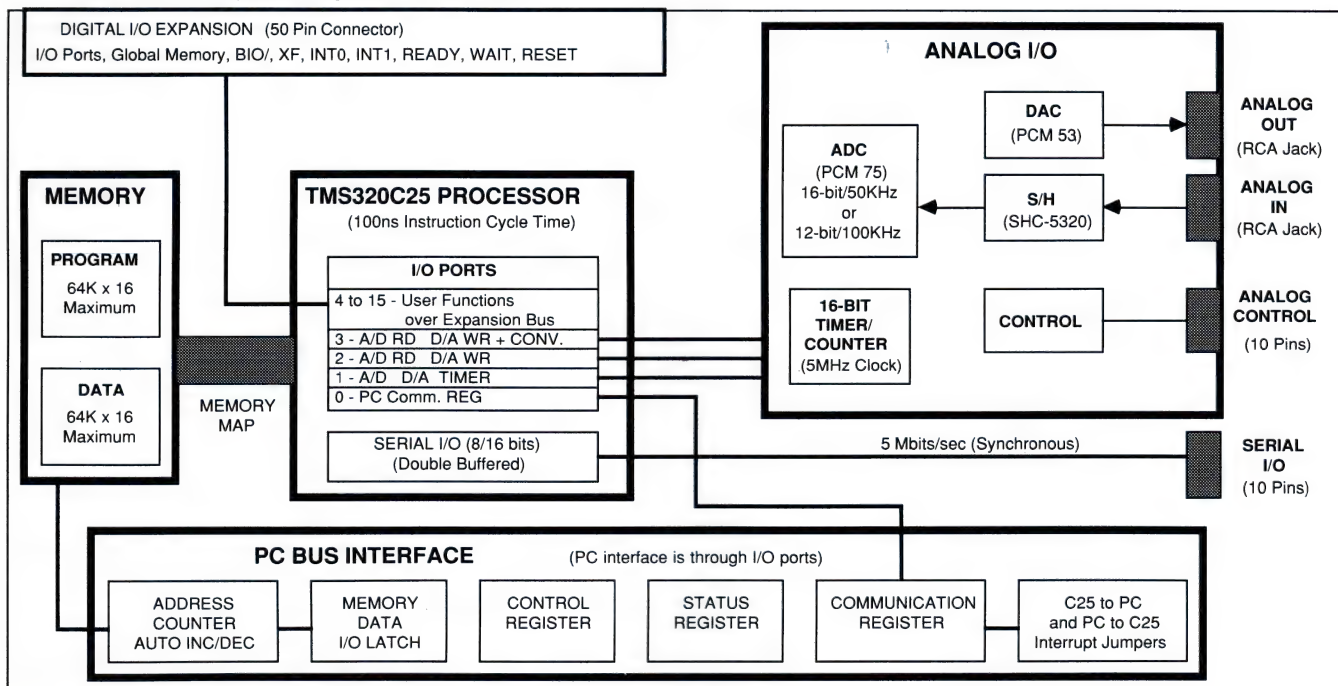
RELATED SOFTWARE PRODUCTS AVAILABLE FROM SPECTRUM

- TI's TMS320C25 Macro Assembler/Linker and 'C' Compiler.
- LSI 'C' Compiler for the TMS320C25 with Linking Assembler.
- **DADiSP** Data Analysis software.
- **DISPRO** Digital Filter Design software.

The following third party products are compatible with the TMS320C25 System Board:

- **Hypersignal-Workstation:** Integrated workstation for signal processing including data acquisition, filtering, frequency domain analysis, and 3D plots.

DSP~LINK System Expansion Interface



• Processor

TMS320C25 running at 40 MHz clock rate.
16-bit processing with 16 x 16 multiplier, 32 bit ALU.
544 words (16 bit) of internal RAM.
8 aux. registers for address pointers & loop counters.
Internal interval timer.

• Memory

System comes with 16 Kwords 35ns RAM (8K program, 8K data).
Supports up to 128K words (16 bit) of on-board memory, link programmable for RAM or EPROM.
Each half of both program and data memory can be independently selected to be 0 wait-state (35ns) or 1 wait-state (100ns) and can contain small (8K x 8) or large (32K x 8) memory devices.
Fast access to memory from PC by inserting one wait-state in the TMS320C25 bus cycle.

• Analog I/O Clocking Options

Main sample clock source is a 16 bit on-board interval timer, clocked at 5 MHz to provide precise time reference down to 76 Hz (clock can be used as processor interrupt).
Software generated sampling can be used.
Internal/external clocking. Internal clock can be output to other boards for synchronous sampling.

• Analog Input

16 bit A/D with sample-and-hold, 54 KHz throughput
Burr-Brown PCM75 (16-bits @ 17μs, 12-bits @ 8.5μs, jumper selectable), Burr-Brown SHC-5320 (1.5μs).
Sample-and-hold can be disabled with jumper.
Voltage range: ± 10V.
Input impedance: 1K ohm.
Type of connector: RCA phono jack on endplate.

• Analog Output

16 bit D/A, Burr-Brown PCM-53 (3μs).
Voltage range: ± 10V.
Output impedance: 1K ohm.
Type of connector: RCA phono jack on end plate.

• PC Interface

8 I/O locations (relocate 8 ways).
Choice of 5 PC interrupts.
Block transfers using auto inc/dec address counters.
16-bit bi-directional communications register with full handshake (polled or interrupt).
8-bit control/status register.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus - master.
Up to 5 Mwords/sec transfer rate.
12 DSP I/O ports available.
Standard 50-pin male header ribbon cable connector.
DSP~LINK specifications are available for interfacing application-specific hardware.

• Serial Interface

5 Mbps, full duplex, internal/external clock and synch, continuous or burst data, 8 or 16-bit data.
Buffered TMS320C25 serial port signals.
Multi-processor capability.
Standard 10-pin header connector (on PC backplate).

• Physical

Full length IBM PC plug-in card.
Dimensions: 13 3/8" L x 4 1/2" H x 5/8" D.

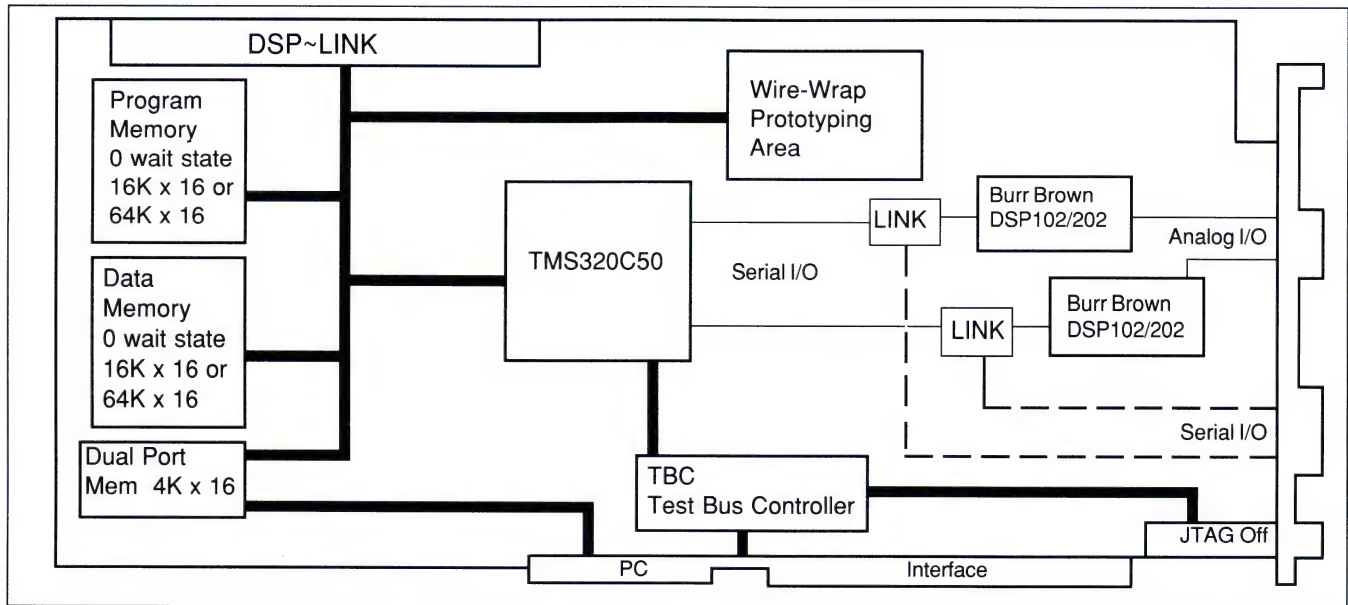
• Electrical

Power consumption: Max: 5V @ 2A
Typ: 5V @ 1.25 A.

TMS320C50 System Board

with Development Support

Part Number: 600-01056
Preliminary Information



FEATURES

- TMS320C50 50ns fixed point Digital Signal Processor.
- DSP~LINK System Expansion Interface.
- 16K x 16-bit Program SRAM expandable to 64K x 16.
- 16K x 16-bit Data SRAM expandable to 64K x 16.
- 4K x 16-bit Dual Port Memory interface to the PC host.
- Dual 200 KHz, 18-bit A/D converters supporting two I/O channels with anti-alias and reconstruction filters.
- Two 10 Mbps serial ports.
- One serial port supports communication with up to seven other TMS320C50 System boards by time division multiplexing.
- Large prototyping area supports user designed peripherals.
- JTAG interface to permit comprehensive debug facilities.
- Windowed monitor/debugger provides sophisticated development capabilities.
- Interface function library callable from Microsoft programming languages.

The TMS320C50 System Board is designed to provide a general purpose digital signal processing system that can be easily controlled via the PC interface. The architecture of the board centers around the Texas Instruments TMS320C50, a general purpose 16-bit fixed point digital signal processor exhibiting very high performance.

The board supports three fast static memory sub-systems external to the TMS320C50 processor. Separate data and program memory areas come equipped with 16K x 16-bits of zero wait state static RAM. Both areas are upgradable to 64K x 16. The other memory area, 4K x 16 bits of dual port memory, is accessible to both the DSP chip and the PC host enabling the PC to access 'C50 data without halting the processor.

Two analog interfaces are included on the board through Burr Brown DSP102/202 devices. These parts provide two channels of A/D and D/A with a 200 KHz sampling rate and 18-bits of resolution. Analog signals with bandwidths of up to 100 KHz can be acquired, processed, and output from the board in real-time. Both 4th order anti-aliasing and reconstruction filters are used.

Two high speed (10 Mbits per second) serial ports permit communication to external devices through a 15 pin D-type connector. One of the serial ports is configured as an eight channel time division multiplexed (TDM) port facilitating communication with up to seven other TMS320C50 System boards.

The TMS320C50 System Board is also equipped with the DSP~LINK system expansion interface. This 50-pin connector permits high speed 16-bit parallel data communications to a range of Spectrum's peripheral interface cards, including a pro-audio interface and high speed transient capture card. DSP~LINK is an "open" architecture suitable for interfacing with a user's own peripheral hardware.

The user prototyping area permits the addition of custom interfaces or expansions. This is particularly useful when taking advantage of the TMS320C50's unique peripheral device support capabilities. All relevant signals (data, address, interrupts) make both the processor and DSP~LINK accessible to user defined circuitry. Spectrum can also provide custom design services and custom boards in production through our "EasyDSP" service.

The TMS320C50 System Board also supports the Texas Instruments JTAG interface. The JTAG scanning logic system provides extensive debug facilities which can be accessed either off-board through a multi-way connector or through the PC bus interface.

DEVELOPMENT SUPPORT

The debug monitor provided is a graphic intensive, windowed format, featuring pull-down menus and mouse support. Debugging features include single step, breakpoint, disassembly, program loading, data upload/download, register inspection/modification and full speed operation.

Sample programs familiarize the user with the TMS320C50 assembly language and give good examples of how a TMS320C50-based system can be used in a PC environment. A library of 'C'-callable board drivers for the PC is provided including 'C' and assembly source code, Microsoft linkable object modules, and several examples.

RELATED SOFTWARE PRODUCTS FROM SPECTRUM

- TI's TMS320C50 Macro Assembler/Linker and 'C' Compiler.
- DADiSP Data Analysis software.
- DISPRO Digital Filter Design software.
- Hypersignal-Workstation: Integrated workstation for signal processing including data acquisition, filtering, frequency domain analysis and 3D plots.

• Processor

TMS320C50 running at 50 MHz clock rate.
16 bit integer arithmetic.
Parallel Logic Unit.
9Kx16-bit prog/data RAM.
2Kx16-bit boot ROM.
1Kx16-bit dual-access RAM.

• Memory

Dual port: 4Kx16-bit, 1 wait-state RAM, dual ported between the C50 and the PC bus.
16Kx16-bit zero wait state program RAM, expandable to 64Kx16-bit.
16Kx16-bit zero wait state data RAM, expandable to 64Kx16-bit.

• Analog Input/Output

Dual 18-bit A/D and D/A converters.
108 dB dynamic range.
Better than 90 dB signal/noise.
THD + noise < 0.005 dB.
200 KHz maximum sample rate triggered by on-board timers or external trigger.
Burr Brown SH5537 S/H circuit on each input.
4th order input and output Butterworth filters, resistor programmable and bypassable.

• Serial I/O

Two 10 Mbit/sec serial ports (hardware link selectable).
One serial port can be configured as an eight channel time division multiplexed (TDM) port to permit communication with up to seven other C50 System Boards.

• Prototyping Area

0.1" grid of holes permitting user designed circuits. Signals allowing direct interface to DSP~LINK and the DSP processor are brought out into the area.

• JTAG Interface

TI's Test bus controller chip enables JTAG boundary scan.
Interface to the PC and external circuitry.

• Interface to PC Host

8-bit PC card format.
Occupies 16 continuous I/O ports.
Choice of 6 PC interrupts.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus.
Up to 5 Mwords/sec transfer rate.
8K memory mapped DSP I/O ports available.
Standard 50-pin male ribbon cable connector.
DSP~LINK specifications are available for interfacing application specific hardware.

• Physical

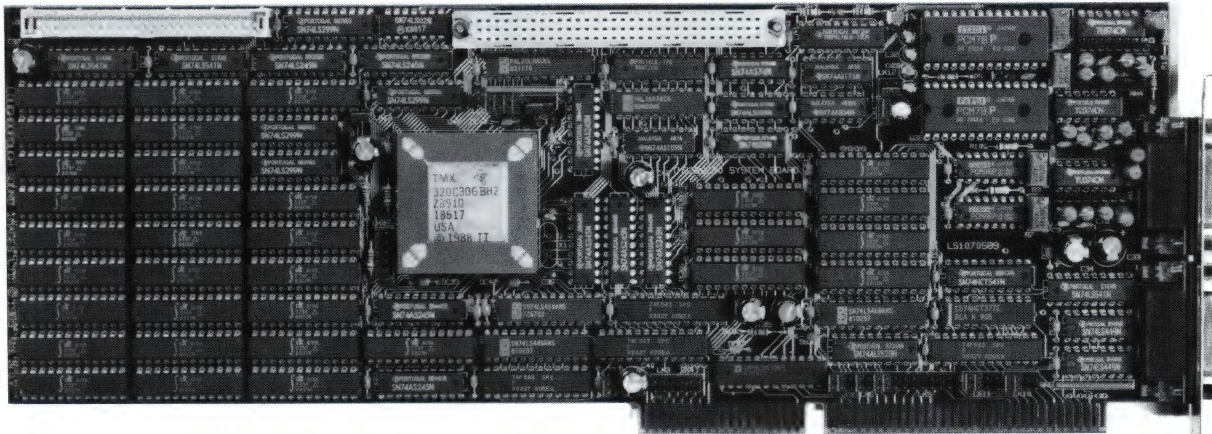
Full length PC plug-in card
Dimensions: 13 3/8" L x 4 1/2" H x 5/8" D.

• Electrical

To be determined.

TMS320C30 Real-Time System with Development Support

Part Number: 600-00554



FEATURES

- TMS320C30 60ns floating point Digital Signal Processor.
- **DSP~LINK** System Expansion Interface.
- 128 Kwords (32-bit) Fast SRAM supplied.
- 256 Kword on-board memory capacity.
- Memory Expansion Connector for future full memory daughter board.
- Two high-speed 16-bit ADCs and DACs.
- Two 8.3 Mbps general purpose serial ports.
- IBM PC/AT 16-bit bus interface with full DMA.
- Monitor software includes single-step, break point, code disassembly and full speed operation.
- SPOX™ DSP operating system and applications interface.
- Interface function library callable from Microsoft programming languages.

The TMS320C30 Real-Time System is a DSP development environment based on Texas Instruments' TMS320C30 60ns floating point DSP coupled with the SPOX™ DSP Operating System.

The hardware is a SPECTRUM TMS320C30 System Board, with two channels of high speed analog I/O on board. Concurrent with other SPECTRUM products, important architectural features of the processor are made available to the user to configure per system requirements. The board supports the C30's 60ns instruction cycle, comes with 128 Kwords of high-speed static ! RAM, upgradable on-board to 256 Kwords. A memory expansion connector provides a means of exploiting the remainder of the C30's 16M memory addressing space by use of a future daughter-board.

I/O mapped, the board occupies 16 locations on the PC/AT 16-bit bus. Also supported are: DMA fast transfers, bi-directional interrupts and multiple board installations.

In addition to two on-board, 150 KHz analog interfaces, data can also be acquired via the **DSP~LINK** system expansion interface. This 50-pin standardized bus is featured on most SPECTRUM products including multi-channel data acquisition cards. This provides the flexibility of tailoring a system for specific analog I/O requirements.

The C30's two high-speed serial ports are fully buffered and extended to a 15-pin D-Type connector for user implementation. Data may be transferred as 8, 16, 24 or 32-bit words, at rates up to 8.3 MHz.

DEVELOPMENT SUPPORT

The debug monitor (for EGA & VGA) provided is a graphic intensive, windowed format, featuring pull-down menus and mouse support. Debugging features include single step, breakpoint, disassembly, program and data transfers, register status and modification, as well as full speed program execution.

Sample programs familiarize the user with TMS320C30 assembly language and provide a programmer's reference for accessing the system's hardware resources. These sample programs include an FFT, a FIR filter, and simple analog I/O functions such as echoing input to output. Source code for these items is included as part of the system documentation.

A library of interface functions callable from Microsoft programming languages is provided to allow easy integration of the DSP application with the PC/AT user interface.

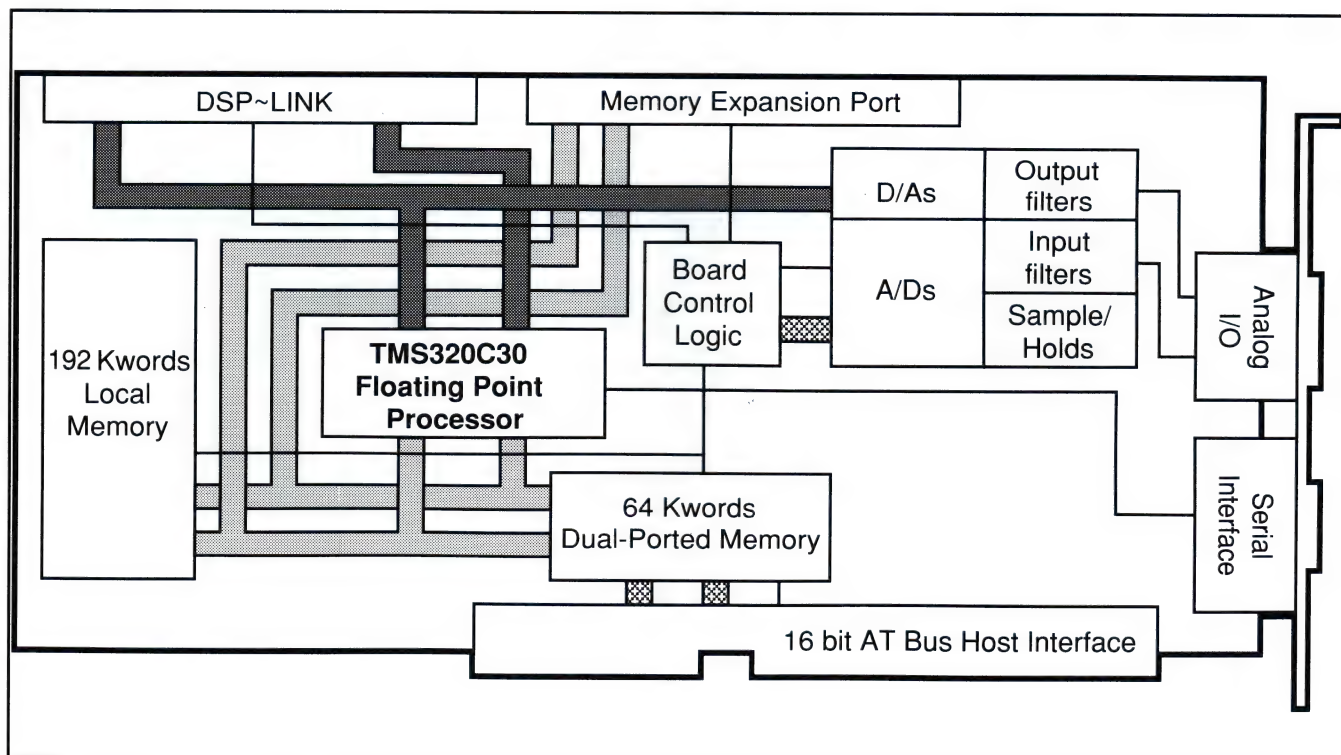
ASSEMBLER/LINKER/C COMPILER & SPOX™

The TMS320C30 Real Time System includes Texas Instruments' Assembler/Linker and C Compiler with SPOX™ as an integral part of the package. High level C language DSP programming is optimized by the SPOX™ operating system.

SPOX™ provides standard I/O support for C so that pre-existing C programs on host computers such as IBM XT or AT will execute with just recompilation. SPOX™ also provides a library of standard DSP system functions which free the user from writing low level code such as device drivers for managing incoming data. Applications written in C, under SPOX™ are portable to other hardware environments supporting SPOX™. SPOX™ also facilitates multi-tasking and multi-processor communications.

RELATED SOFTWARE PRODUCTS AVAILABLE FROM SPECTRUM

- T.I. TMS320C30 Assembler/Linker sold separately.
- DADiSP Data Analysis software.
- Hypersignal-Workstation:
Integrated workstation for signal processing including data acquisition, filtering, frequency domain analysis, and 3D plots.



- **Processor**

TMS320C30 running at a 33.33 MHz clock rate (60ns instruction cycle).
32-bit floating point arithmetic.
Eight 40-bit accumulators.
2 Kwords dual access RAM.
4 Kwords dual access ROM.

- **Memory**

Dual port: 64K X 32, 1 wait-state (35ns) RAM, dual ported between the C30 and the PC bus.
C30 Local: 64K X 32, 0 wait-state (25ns) RAM, expandable to 192K X 32.
Off Board: Memory expansion connector facilitates off-board expansion to full C30 capacity.

- **Analog Input**

Two 16-bit ADCs with sample-and-hold, 153KHz throughput [Burr-Brown PCM78 (5us), Burr-Brown SHC5320 (1.5us)].
Fourth order filters.
Double-buffered data latching.
Voltage range: $\pm 3V$.
Connections: DB15 style

- **Analog Output**

Two 16-bit DACs [Burr-Brown PCM56 (1.5us)].
Fourth-order filters.
Double-buffered data latching.
Voltage range: $\pm 3V$.
Connections: DB15 Style.

- **Analog I/O Clocking Options**

Software initiated conversions.
C30 on-chip timer initiated conversions
External trigger pulses.

- **Serial I/O**

Two synchronous 8.3 Mbps serial ports.
All signals buffered.
Fully configurable for global compatibility.

- **Interface to PC Host**

16-bit PC/AT card format.
Occupies 16 contiguous I/O ports (fully mappable).
Choice of six PC interrupts.

- **DSP~LINK System Expansion Interface**

16-bit parallel expansion bus.
Up to 5 Mwords/sec transfer rate.
8K memory-mapped DSP I/O ports available.
Standard 50-pin male ribbon cable connector.
DSP~LINK specifications are available for interfacing application-specific hardware.

- **Physical**

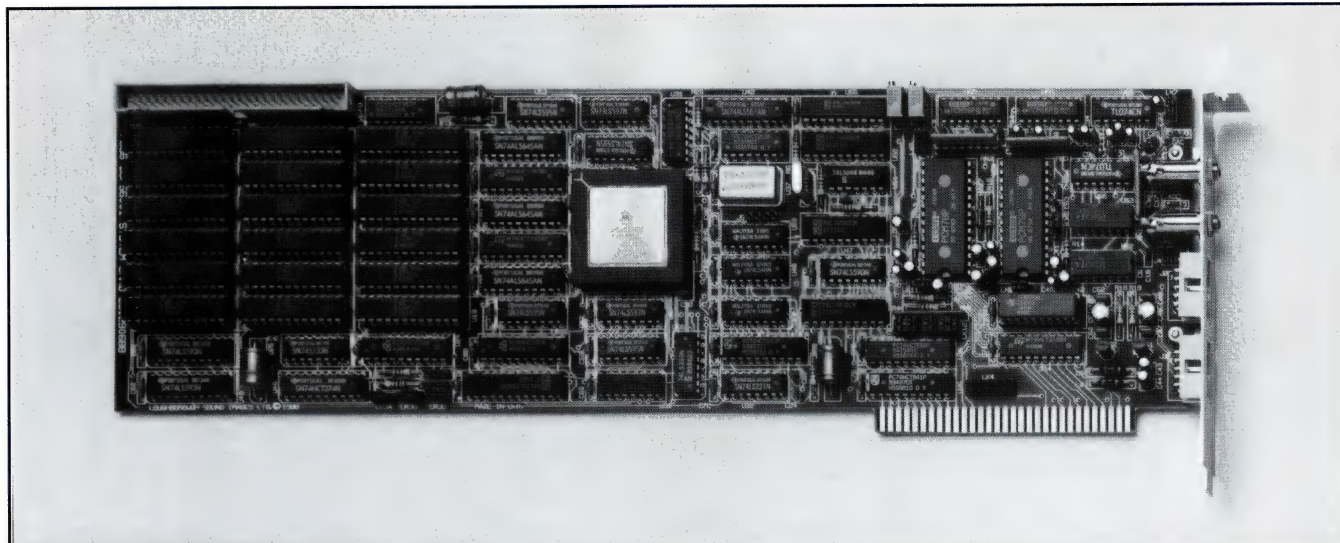
Full length PC/AT plug-in board.
Dimensions: 13 3/8"L x 4 5/8"H x 5/8"D.

- **Electrical**

Power consumption: 5V @ 2.0A, 12V @ 150 mA,
-12V @ 150mA

DSP56001 System Board with Development Support

Part Number: 600-00202



FEATURES

- Motorola 56001 24-bit 100ns processor.
- **DSP~LINK** System Expansion Interface.
- 192 Kwords of on-board memory capacity.
- Two high-speed 16-bit ADCs and DACs.
- COMBO/CODEC analog interface for telecom.
- Two high-speed serial I/O channels.
- IBM-PC/XT/AT or true compatible plug-in board.
- Monitor software including single step, breakpoint and full-speed operation.
- 'C' Board drivers.

The DSP56001 System Board offers a general purpose DSP architecture with the optimization and performance of Motorola's "fourth generation" processor.

The system runs with a 100ns instruction cycle and comes with 48 Kwords of 35ns static RAM for zero wait-state operation. Host access to system memory, peripherals and registers is achieved using the 56001's specialized host/DMA interface. The interface appears to the host (PC) as a block of sixteen locations in its I/O address space.

In addition to the on-board analog interfaces, data can also be acquired via the **DSP~LINK** system expansion interface. This 50-pin standardized expansion bus is featured on all SPECTRUM products including multi-channel data acquisition cards, providing users with the flexibility of tailoring a system to match their analog and digital I/O requirements.

Two full duplex serial ports are provided, one synchronous and one asynchronous. The SSI port has its signals available on a connector at the rear of the PC.

SPECTRUM provides a similar board without analog I/O called the "DSP56001 Processor Board". Please refer to the appropriate data sheet for information on this product.

DEVELOPMENT SUPPORT

Debug monitor software is provided in two forms. A simple, command-driven version and a window-based menu-driven version. Its features include memory-register examination and modification, program downloading, disassembly, single step, and multiple event-counting breakpoints.

Sample programs familiarize the user with DSP56001 Assembly language and give good examples of how a DSP56001-based system can be used in a PC environment. These sample programs include a 1024-point FFT, a FIR filter and a data logger. Source code for these items is included as part of the system documentation.

A library of 'C'- callable board drivers for the PC is provided including 'C' and assembly source code, MICROSOFT linkable object modules, and many examples.

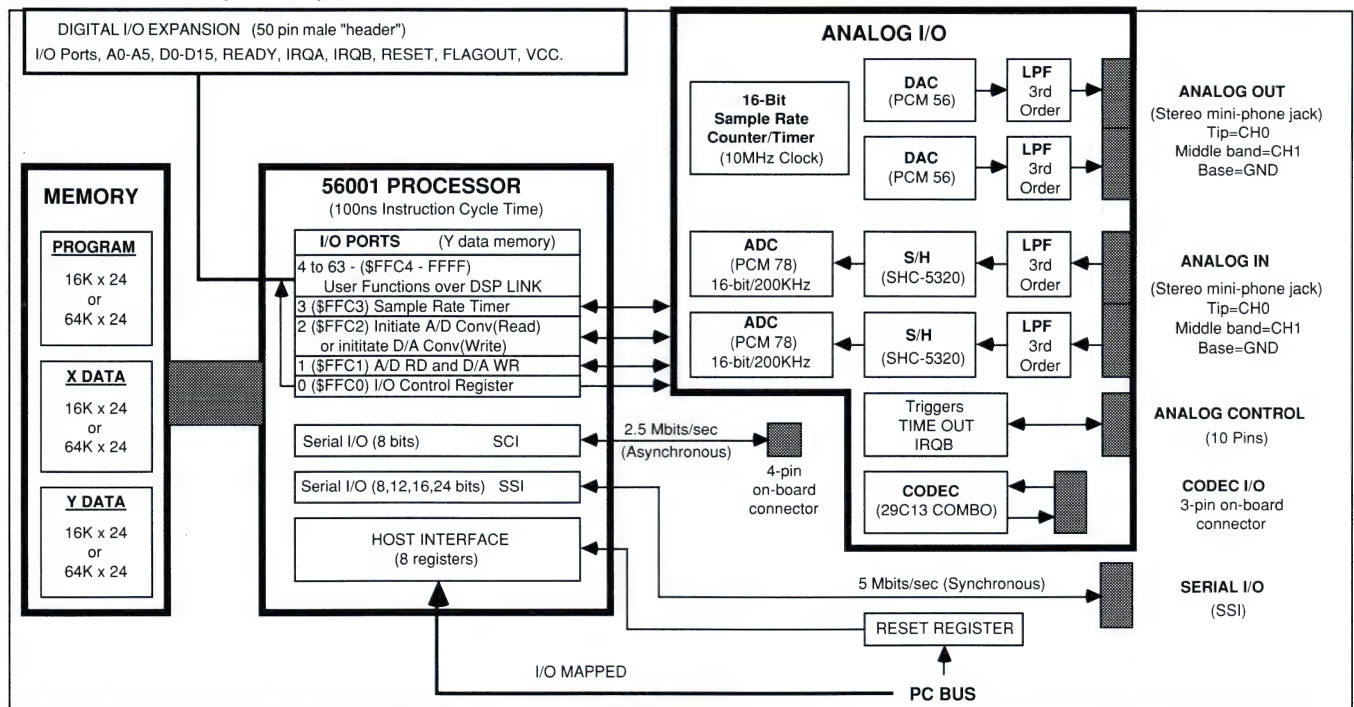
RELATED SOFTWARE PRODUCTS AVAILABLE FROM SPECTRUM

- Motorola DSP56000CLASx Assembler/Simulator.
- Motorola DSP56KCCx 'C' Language Compiler.
- **DADISP** Data Analysis software.
- **DISPRO** Digital Filter Design software.

The following third party products are compatible with the DSP56001 System Board:

- **Hypersignal-Workstation:** Integrated workstation for signal processing including data acquisition, filtering, frequency domain analysis, and 3D plots.
- **Momentum** Filter Design and Analysis software with Code Generator.

DSP~LINK System Expansion Interface



• Processor

56001 at 20 MHz clock rate (100ns instruction cycle).
24-bit processing with 24 x 24 hardware multiplier and two 56-bit accumulators.
512 words (24-bit) internal data RAM.
512 words (24-bit) internal program RAM.
Four (4) data busses.
Internal ROM contains μ law/A-law to linear and sine tables.

• Memory

System comes with 48K x 24 of 35ns RAM (16K x 24 in each of PGM, X, and Y).
Supports up to 192K x 24 of on-board memory (64K x 24 in each of PGM, X, and Y).
Software selectable wait-states for slower RAM/EPROM.

• Analog Inputs

Two 16-bit ADCs with sample-and-hold, 153KHz throughput [Burr-Brown PCM78 (5us) and SHC-5320 (1.5us)].
Third order filtering (resistor programmable).
Double-buffered data latching.
Voltage range: $\pm 3V$.
Type of connectors: 3.5mm stereo jacks.

• Analog Outputs

Two 16-bit DACs [Burr-Brown PCM56 (1.5us)].
Third order filtering (resistor programmable).
Double-buffered data latching.
Voltage range: $\pm 3V$.
Type of connector: 3.5mm stereo jacks.

• Analog I/O Clocking Options

Software-initiated conversions.
16-bit timer initiated (minimum sample rate 153Hz).
External trigger (endplate).

Timer and external triggering can interrupt 56001.

• Serial I/O

Two I/O channels with internal/external clocks.
Synchronous (SSI) 5.0MHz with 10-pin connector on end plate.
Asynchronous (SCI) 2.5MHz with 4-pin connector on-board.

• Telecom Interface

Intel 29C13 "Combo" CODEC (μ -law/A-law).
Uses synchronous serial interface.
I/O via 3-pin connector or 3.5mm stereo jack.

• Interface to PC Host

56001 host/DMA interface mapped into a block of 16 I/O locations in the PC.
On-chip integration of this interface provides low overhead access to registers, memories, and peripherals.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus - master.
Up to 5 MWords/sec transfer rate.
60 DSP I/O ports available (Y: FF04-FFFF).
2 DSP interrupts.
Standard 50-pin male header ribbon cable connector.
DSP~LINK specifications are available for interfacing application-specific hardware.

• Physical

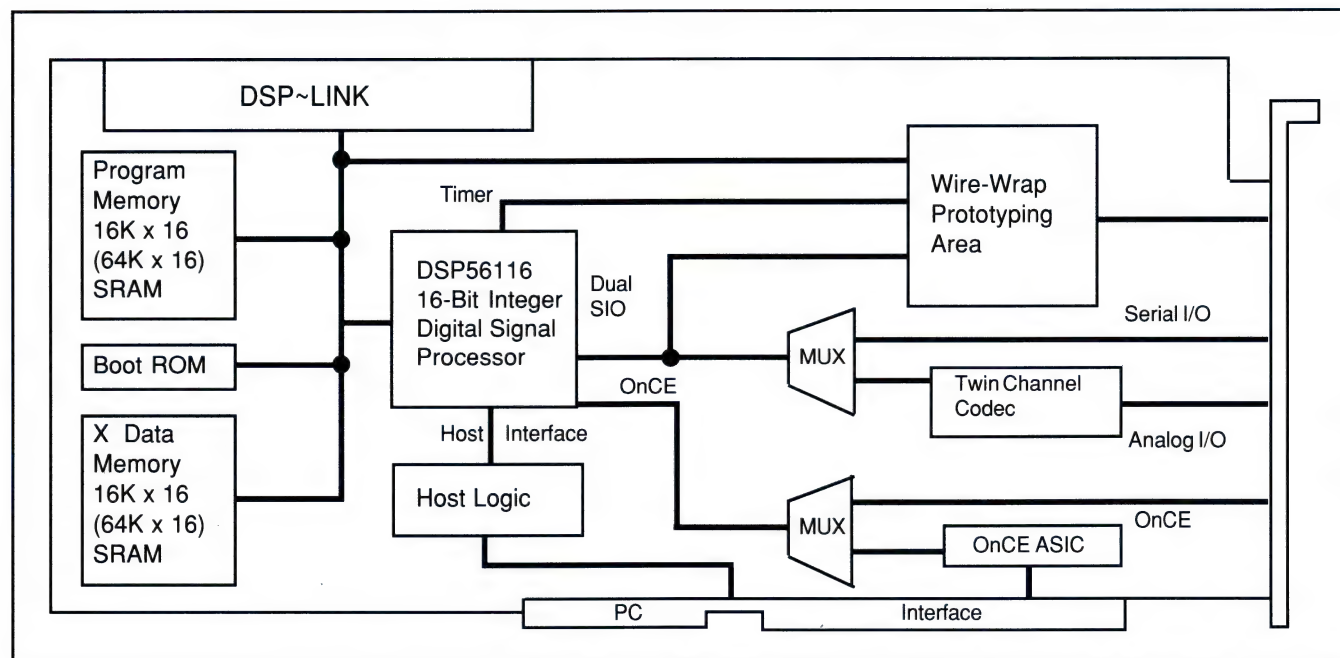
Full-length IBM-PC plug-in card.
Dimensions: 13-3/8" L x 4-1/2" H x 5/8" D.

• Electrical

Power consumption: 5V @ 2A max.

DSP56116 System Board with Development Support

Part Number: 600-01101
Preliminary Information



FEATURES

- Motorola DSP56116 16-bit 80 MHz Processor.
- DSP-LINK System Expansion Interface.
- Up to 128 Kwords of 0 Wait State on-board memory.
- BOOT ROM for Standalone Operation.
- Twin CODECs provide a Telecom Based Interface.
- Dual Synchronous Serial Port.
- Large Wire-Wrap Prototyping Area for User Custom Circuitry.
- On-Board OnCE Interface Circuit.
- Fast PC Data Transfer via Host Interface.
- Command Line Based and Windows 3.0 Based Debug Tools.

The DSP56116 System Board offers a unique, high performance DSP architecture ideally suited to telecommunications, speech, and audio control systems.

Based on the Motorola DSP56116, a high performance 16-bit integer digital signal processor, the system is capable of delivering 40 MIPS of processing power. The board also comes with 30 Kwords of 0 wait-state 12ns SRAM (16 Kwords Program/ 14 Kwords X Data), expandable up to 128 Kwords of 0 wait-state SRAM.

The board is equipped with two CODECs for 2-channel Analog I/O, and are connected to the two serial ports of the DSP56116. The CODECs can be easily disconnected by changing links, making the two serial ports available to the user prototype area (unbuffered) or the external serial I/O connector (buffered), both of which are described below.

A large wire-wrap prototyping area included on the DSP56116 System Board allows user defined peripherals to be directly

accessed by the DSP56116. The area is mapped into 512 memory locations of the X data memory address range and the DSP56116's Port B (Host Interface) and Port C (Serial Interface) are brought out unbuffered to this area. In addition, the prototype area is equipped with buffered X Data lines D0-D15 and address lines A0-A8 (512 words), with memory access times of 50ns (address range FA00-FBFF) and 150ns (address range F800-F9FF). An external wait state generator controls the memory access time.

The DSP56116 System Board provides dual synchronous serial ports capable of operating at 20 Mbits/sec. The ports are multiplexed via links between the two CODECs, and are buffered to drive external serial I/O devices via a D-type socket. An unbuffered version of the signals is also made available to the user prototype area.

In addition to the CODEC based analog I/O, the board is also equipped with Spectrum's DSP-LINK. This standardized, bidirectional 16 bit expansion interface supports high-speed parallel data communications over a 50-pin ribbon cable connector. DSP-LINK provides a fast link to a wide range of peripheral interface cards including multi-channel data-acquisition cards, a digital pro-audio interface card, and a card for high speed transient capture. DSP-LINK is an "open" architecture, suitable for interfacing with a user's own peripheral hardware. All the necessary data, address, and control lines are provided.

The board makes use of the DSP56116 Host Interface for communication between the DSP and the PC. This facilitates the downloading of programs to the on-board Program Memory and the reading and writing of data to the on-board X Data Memory. The Host Interface is memory mapped into the PC I/O space.

The DSP56116 can boot from either the PC Interface, the serial port, or a boot ROM. The board normally boots from the PC Interface, but has the provision for a 27C64 boot ROM to allow stand-alone operation, selectable via links. The 27C64 can store 2 x 4K byte pages of memory, each of which can store a boot program, selectable via links.

DEVELOPMENT SUPPORT

The DSP56116 System Board supports Motorola's OnCE™ on-chip emulation capability, resulting in no additional debugging hardware. The DSP56116 OnCE circuit interacts with any memory peripheral, permitting users to examine registers, memory, and the on-chip/off-chip peripherals of an embedded DSP56116 while maintaining full debug control - without the need for on-chip resources.

The OnCE interface is supported with a command line monitor debugger and WINDOWS56116, a Microsoft Windows 3.0 based symbolic debugger. Both use the DSP56116's on-chip OnCE debug circuitry to perform single stepping, display/modification of all registers and memory, disassembly, command macros and full speed execution with or without software breakpoints.

Sample programs familiarize the user with DSP56116 Assembly language programming and give excellent examples of how a DSP56116 based system can be used in a PC environment. Source code for these programs is included as part of the system documentation.

Motorola's DSP56116/CLASx support software including assembler, linker/librarian, and simulator are also available separately from SPECTRUM.

• Processor

Motorola DSP56116 running at 80 MHz.
16-bit integer architecture.
Single-cycle 16x16-bit parallel multiply-accumulator.
Two 40-bit accumulators.
2 Kwords of Internal X Data Memory.
2 Kwords of Internal Program Memory.
64 Kword X Data Memory Range.
64 Kword Program Memory Range.
On-Chip Emulation (OnCE) Interface.

• Memory

Program:
16 Kwords of 0 wait state (12ns) Static RAM,
expandable up to 64 Kwords.
X Data:
14 Kwords of 0 wait state (12ns) Static RAM,
expandable up to 62 Kwords.

• Analog I/O

Two CODECs for two channels of analog I/O.
Each CODEC is connected to one of the DSP56116 serial ports.

• Serial I/O

20 Mbps Dual synchronous serial ports.
Multiplexed via links between CODECs and a D-type Socket.
Unbuffered signals are available to the prototype area.

• Interface to PC Host

The DSP56116 Host Interface is used for DSP to PC Communication and is memory mapped into the PC I/O address space.

• DSP-LINK System Expansion Interface

16-bit parallel bidirectional expansion bus.
Up to 5 Mwords/sec bus transfer rate.
448 DSP I/O ports available (X:FC00-FFBF).
Standard 50-pin male header ribbon cable connector.
DSP-LINK specifications are available for interfacing application-specific hardware.

• Physical

Full length PC/AT plug-in board.
Dimensions: 13-3/8"L x 4-5/8"H x 5/8"D.

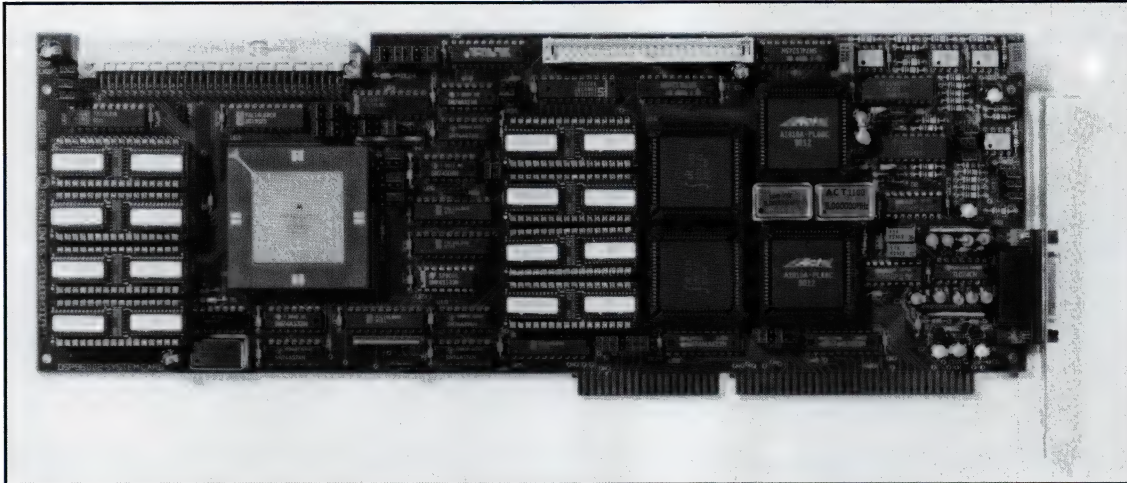
• Electrical

To be Determined.

DSP96002 System Board

with Development Support

Part Number: 600-00993
Preliminary Information



FEATURES

- 33 MHz Motorola DSP96002 with 16.7 MIPs and 50 MFLOPs throughput
- Supplied with 64 Kwords of zero-wait state memory and 256 Kwords of 1 wait-state memory, user expandable to an on-board maximum of 1088 Kwords
- 2 Kwords memory dual ported to the PC
- Dual delta sigma 16 bit A/D and D/A channels
- MOTOWAY multi-processor expansion connector
- DSP~LINK expansion port
- Library of 'C' callable board drivers
- Monitor debugger

The DSP96002 System Board is an IBM PC plug-in board designed to support algorithm development and applications based on Motorola's DSP96002, a dual port, IEEE floating point digital signal processor.

The standard memory configuration is a bank of 32 Kwords of zero wait-state and 128 Kwords of 1 wait-state SRAM mapped to each DSP96002 port. Each bank is expandable by a further 384 Kwords using 1wait-state devices to form a contiguous block of 544 Kwords. The memory can be configured in both overlay and non-overlay modes. The non-overlay mode allows the memory to be split into three areas, P, X, and Y; all starting at the same address. The overlay mode requires the user to explicitly partition the memory in software for the P, X, and Y areas.

Efficient data transfers to and from the PC are facilitated using 2 Kwords of dual-port memory. Mapped into portA of the DSP96002, this memory appears as an 8 Kbyte block in the memory map of the PC (link selectable from 80000h to FE0000h). DMA transfers between the 96002 memory and the dual ported memory are easily performed and can be in either the fastest time possible, or with no delays to the 96002's processing.

Two Motorola DSP56ADC16 delta sigma A-to-D converters

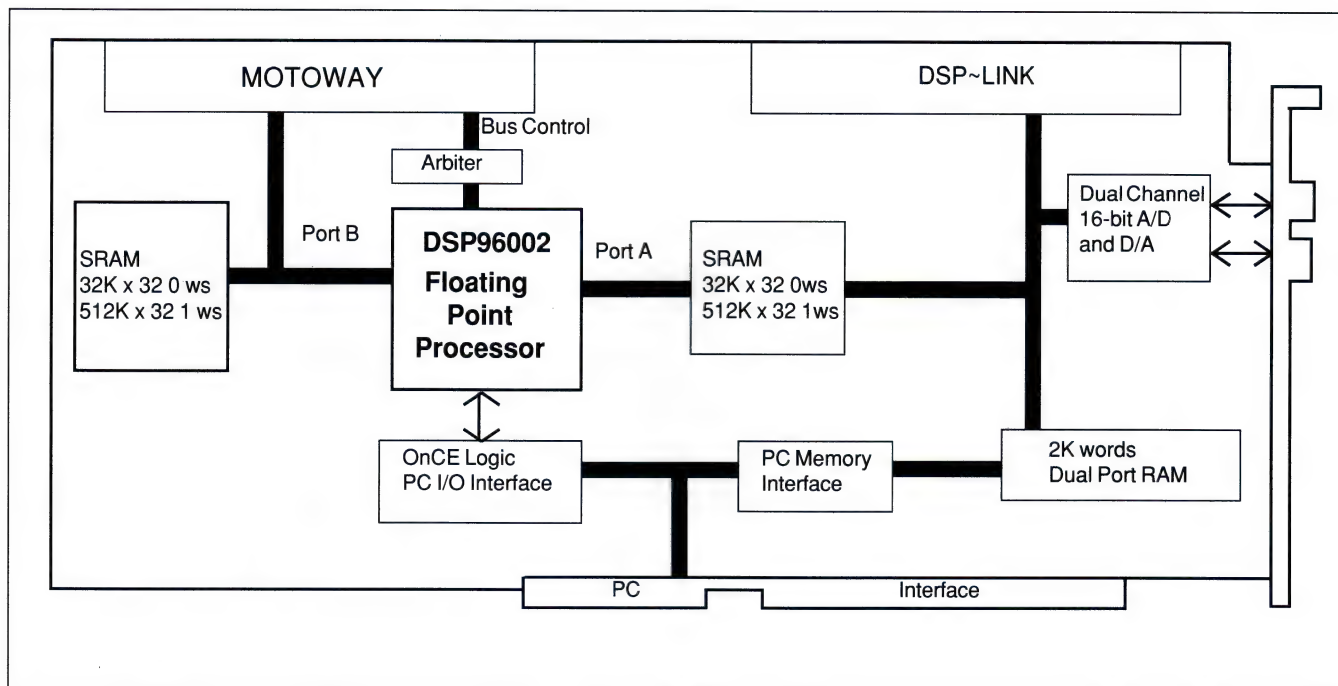
provide an analog input capability. These devices operate on an oversampling basis and incorporate high quality digital anti-aliasing filters which automatically compensate for sampling frequency changes. The sampling frequency is software selectable from 8 to 100 KHz at 16-bits resolution and up to 400 KHz at 12-bits resolution. Two 16-bit Burr-Brown PCM56 DACs and 4th order Butterworth reconstruction filters provide stereo analog output.

In addition to the on-board analog interfaces, data can also be acquired via the DSP~LINK system expansion interface. This 50-pin standardized expansion bus, available on all SPECTRUM products, allows users to configure a system to match their analog and/or digital I/O requirements.

The 96-way MOTOWAY expansion connector allows up to four DSP96002 System Boards to be directly connected in a true multi-processing configuration. The arbitration logic on each board allows any one of the four DSP96002s to be the bus master on a round robin basis, with the possibility of adding additional slave boards. When a DSP96002 System Board becomes the bus master, it can directly access, via the host interface, any portB SRAM in the system and indirectly access the resources connected to portA of any other system board. In order to provide a fast, efficient, and reliable method of inter-connecting multiple DSP96002 System Boards, a multi-layer, terminated backplane is available. MOTOWAY can also provide expansion capabilities for a single DSP96002 System Board.

DEVELOPMENT SUPPORT

The DSP96002 System Board requires no additional hardware for debugging. It is supported with a command line monitor debugger and WINDOWS96, a Microsoft Windows 3.0 based symbolic debugger. Both use the DSP96002's on-chip OnCE debug circuitry to perform single stepping, display/modification of all registers and memory, disassembly, command macros and full speed execution with or without software breakpoints.



Sample programs familiarize the user with program development and how the system can be used in a PC environment. A library of 'C'-callable board drivers for the PC is provided including 'C' and assembler source code and Microsoft linkable object code.

Motorola's DSP96002/CLASx support software including assembler, linker/librarian, C compiler, and simulator is available separately from SPECTRUM. Intermetrics' InterTools 96002 software development package including an optimizing C compiler,

a Motorola-compatible macro assembler, utility programs (run-time library routines, formatter, linker-locator, ROM processor, global symbol map, symbol list and librarian) and XDB, a source level cross debugger, is also available separately from SPECTRUM.

The SPOX™ real-time operating system from Spectron Microsystems and Hypersignal-Workstation from Hyperception are currently being ported for the DSP96002. SPECTRUM will offer these application tools as soon as they become available.

• Processor

Motorola DSP96002 running at 33 MHz (60 ns instruction cycle)
IEEE 32-bit floating point architecture
512 words RAM and 32 words ROM in program memory
512 words RAM and 512 words ROM in each of X and Y data memory
On-chip emulator interface (OnCE)

• Memory

PortA: 32K x 32, 0 wait-state and 128K x 32, 1 wait-state, expandable to a maximum of 544K x 32
PortB: 32K x 32, 0 wait-state and 128K x 32, 1 wait-state, expandable to a maximum of 544K x 32
Dual Port to PC: 2K x 32, 1 wait-state

• Analog Inputs

Two 16-bit ADCs, Motorola DSP56ADC16 delta sigma
Double buffered data latching
100 KHz/channel throughput at 16-bits resolution
400 KHz/channel throughput at 12-bits resolution

• Analog Outputs

Two 16-bit DACs, Burr-Brown PCM56 (1.5 us)

Fourth-order reconstruction filters
Double buffered data latching
Voltage range: +/- 3 volts

• Analog I/O Clocking Options

Software initiated

• Interface to PC Host

OnCE port mapped to 16 PC I/O ports.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus
5 Mwords/sec maximum bus transfer rate
Standard 50-pin male header ribbon connector
DSP~LINK specifications are available for interfacing to custom hardware

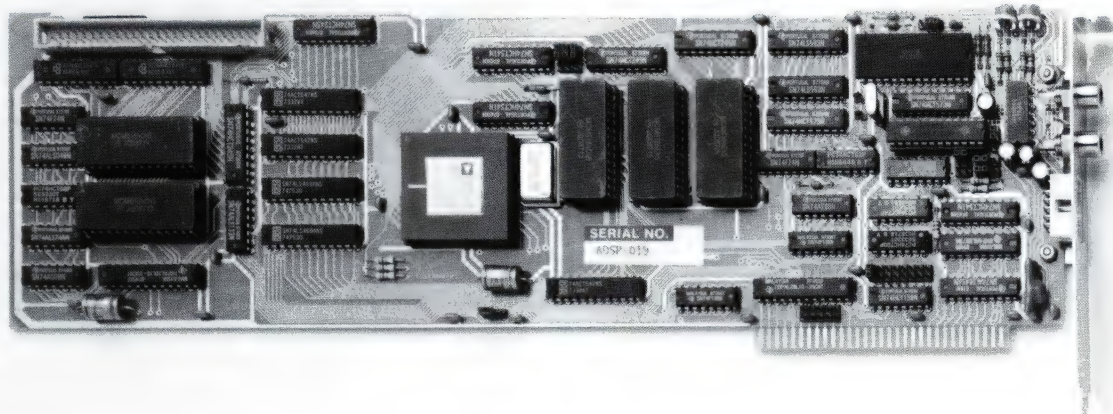
• MOTOWAY System Expansion Interface

• Physical

Full-length IBM PC plug-in board.
Dimensions: 13-3/8"L x 4-5/8"H x 5/8"D

• Electrical

Power consumption: to be tested



FEATURES

- ADSP-2100A 16/24-bit Processor.
- **DSP~LINK** System Expansion Interface.
- High Speed 200KHz 12-bit A/D and D/A.
- Sample-and-hold on input.
- On-board interval timer.
- 40 Kwords on-board memory capacity.
- IBM PC, XT, AT plug-in board.
- Debug Monitor Software supports breakpoints, register examination, and full speed operation.
- 'C' board drivers.

The system runs at full speed (100ns instruction cycle) and comes with 16 Kwords of 35ns static RAM for zero wait-state operation. All DSP memory is dual-access with the PC, allowing automatic host access while the DSP is running.

The ADSP-2100 System Board is I/O mapped and occupies just eight locations of the PC's I/O address space. These include a 16 bit bi-directional data port, control and status register, and a 16-bit loadable address register/counter. The system can also generate and receive interrupts.

In addition to the on-board analog interface, data can also be acquired via the **DSP~LINK** system expansion interface. This 50-pin standardized expansion bus is featured on most SPECTRUM products including multi-channel data acquisition cards, providing users with the flexibility of tailoring a system to match its analog and/or digital I/O requirements.

DEVELOPMENT SUPPORT

The debug monitor software provides the same user interface as Analog Devices' Software Simulator, and can output data in the Simulator's format. This monitor supports symbolic debugging, full speed execution with or without software breakpoints, single stepping, display/modification of all registers

and memory, a disassembler, hardware benchmark timing, command macros, and many other features. ADSP-2100 assembly code is also provided for a 1024-point complex FFT, IIR and FIR filters, and I/O functions.

A library of 'C'- callable board drivers for the PC is provided including 'C' and assembly source code, MICROSOFT linkable object modules, and many examples.

RELATED SOFTWARE PRODUCTS AVAILABLE FROM SPECTRUM

Analog Devices' ADSP-2100 development tools include:

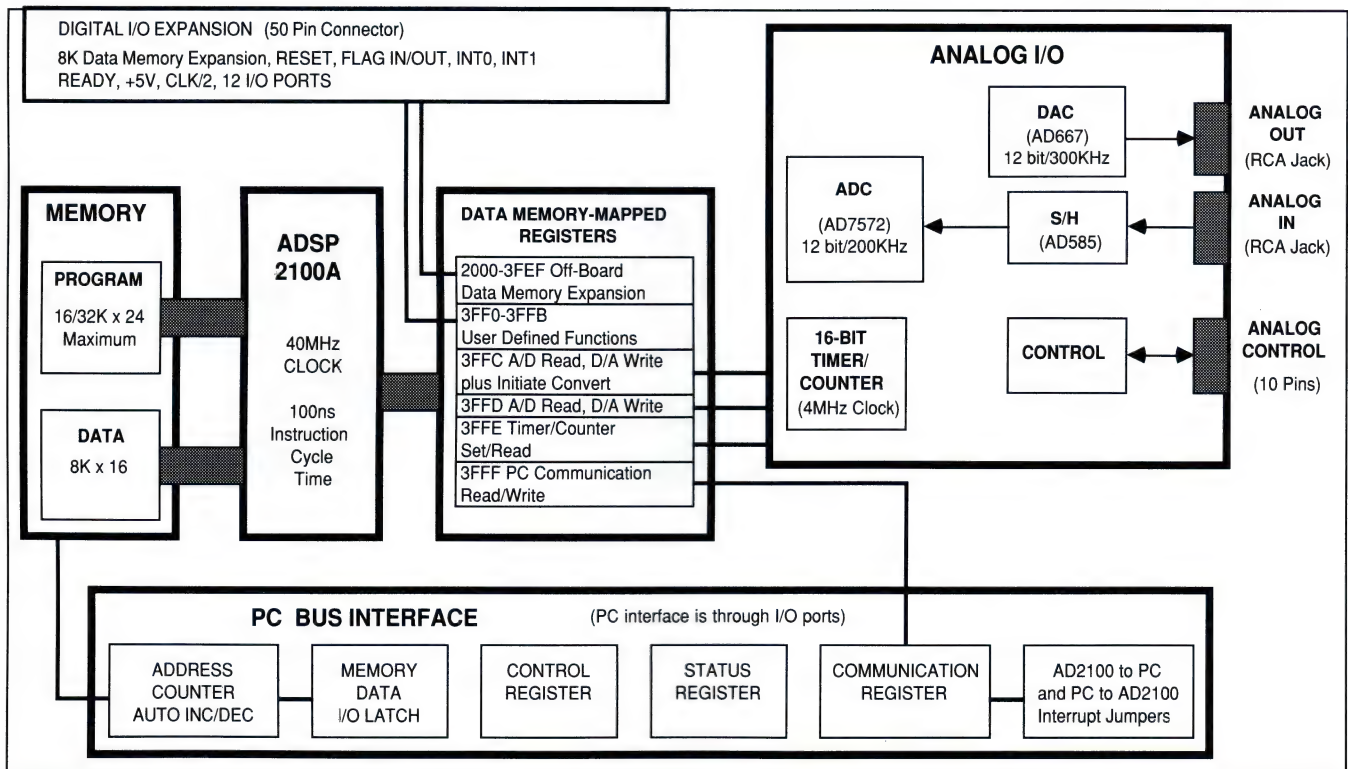
- **Cross-Software Suite** with System Builder, Assembler/Linker, PROM splitter, and Simulator.
- **'C' Compiler.**

The System Builder generates a specification of the target hardware environment, which supplies the other development modules with the details they require to assemble, link and run code. The Assembler/Linker supports the high level syntax of the instruction set and provides a full range of diagnostics. The PROM splitter reads the Linker output and generates PROM burner compatible files in a variety of industry standard formats.

The Simulator, using the output from the System Builder, assumes the architecture of the user's design, and provides several execution modes, including Emulator mode and Single Step. It has six major display modes and a wide variety of utilities and functions.

- **DADiSP** Data Analysis software.
- **DISPRO** Digital Filter Design software.

DSP~LINK System Expansion Interface



• Processor

ADSP 2100A running at 40 MHz with independent ALU, 16 x 16 multiplier, 40-bit accumulator, & barrel shifter. 2 physically separate, off-chip memory busses. Instruction cache memory provides performance equivalent to three memory system. Hardware aids implementation of block floating point.

• Memory

System comes with 8 Kwords (24 bit) program/data memory and 8 Kwords (16 bit) data memory. The former is expandable to 32 Kwords. The latter, to 16 Kwords, off-board only. All supplied RAM is 35ns, for zero wait-state operation.

• Analog I/O Clocking Options

Main clock source for A/D & D/A is a 16-bit on-board interval timer, clocked at 5MHz, providing sample rates down to 76 Hz. Software generated sampling can be used. External clocking is available using the Analog Control Connector.

• Analog Input

12-bit A/D with sample-and-hold, 125KHz throughput, Analog Devices AD7572 (5μs) and AD585 (3μs). Voltage range: ±2.5V. Input impedance: 20K ohms. Type of connector: RCA phono jack on endplate.

• Analog Output

12 bit D/A, Analog Devices AD667 (3μs). Voltage range: ±2.5V or ±5V (at ± 5mA). Output impedance: 0.05 ohms. Type of connector: RCA phono jack on endplate.

• Interface to PC Host

All PC access achieved using just 8 I/O addresses. Interface uses loadable address register/counter, enabling fast, low overhead block transfers. Messages can be passed via a 16 bit bi-directional port, for which interrupts can be generated in either direction.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus - master. Up to 5 Mwords/sec transfer rate. 4 of 16 DSP peripheral addresses used. Standard 50-pin male header ribbon cable connector. DSP~LINK specifications are available for interfacing application-specific hardware.

• Physical

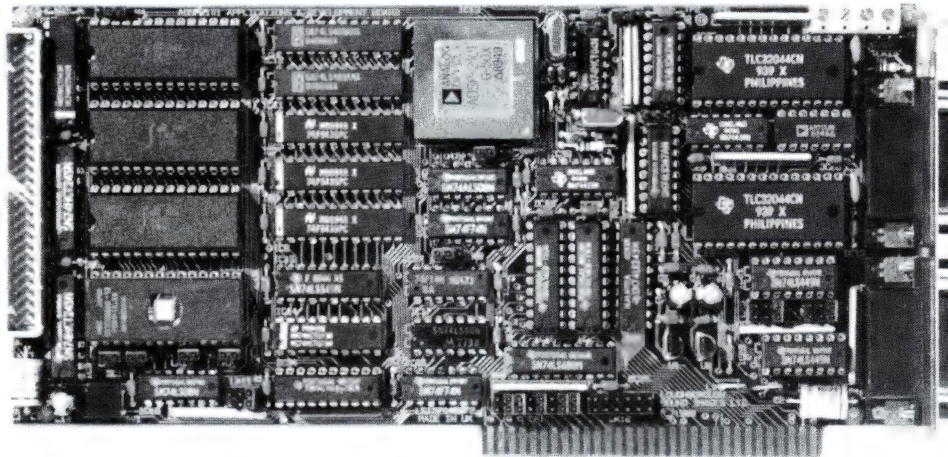
Full length IBM PC plug-in card. Dimensions: 13 3/8" L x 4 1/2" H x 5/8" D.

• Electrical

Power consumption:
Typical: +5V @ 750mA, +12V @ 20mA, -12V @ 30mA.
Maximum: +5 V @ 1A.

ADSP-2101 System Board with Development Support

Part Number: 600-00671



FEATURES

- ADSP-2101 16/24-bit 80ns Processor.
- **DSP~LINK** System Expansion Interface.
- 4K Words (24-bit) of program memory expandable to 14K Words.
- 4K Words (16-bit) of data memory expandable to 12K Words.
- Socket for 32K Byte EPROM for user code in stand-alone mode.
- Dual 19.2 KHz codecs (14-bit) supporting two I/O channels with anti-alias and reconstruction filters, and $(\sin x)/x$ correction.
- Two 6.25 Mbs serial I/O ports.
- IBM PC, XT, AT plug-in board.
- Debug Monitor Software supports breakpoints, register examinations, and full speed operation.
- 'C' board drivers.

The system runs at full speed (80ns instruction cycle) and comes with 4K Words of 24-bit program memory and 4K Words of 16-bit data memory. All DSP memory is 35ns zero wait-state and dual-access with the PC, allowing automatic host access while the DSP is running.

The ADSP-2101 System Board is I/O mapped and occupies just eight locations of the PC's I/O address space. Users may configure up to 8 boards in one PC. The I/O ports include a 16-bit bi-directional communications register, control and status registers, memory address up/down counter register, and a memory data register. The system can also generate and receive interrupts.

To facilitate installation in actual end-use equipment, the board can be configured to operate in a stand-alone mode. In stand-alone mode, the DSP program can be "booted" from an on-board EPROM. If the board is put into stand-alone mode while still physically inside the PC chassis, the PC can communicate with the board, but is relieved from the task of initializing the board. Alternatively, the board can be completely removed from the PC environment and placed inside the user's custom equipment. To assist with this, there are four mounting holes in each corner of the board, a manual reset switch, and a separate power input connector with screw terminals.

Dual codecs with 14-bit dynamic range provide two independent analog I/O channels. Sampling rates up to 19.2 KHz for both single-ended and differential I/O signals are supported. Each codec contains an 8th order Chebyshev/elliptic translational, switched capacitor, anti-alias filter, a 4th order high pass filter that can be switched in or out under software control, a reconstruction filter, and $(\sin x)/x$ correction.

In addition to the on-board analog interface, data can also be acquired via the **DSP~LINK** system expansion interface. This 50-pin standardized expansion bus is featured on most SPECTRUM products including multi-channel data acquisition cards, providing users with the flexibility of tailoring a system to match its analog and/or digital I/O requirements.

Two independent full duplex serial ports are buffered and brought out to DB15 style connectors. Each port is available only when its corresponding codec is not in use. Word lengths of 3 to 16 bits and sample rates of up to 6.25 Mbits per second (or 12.5 Mbits per second with an external clock) are supported.

DEVELOPMENT SUPPORT

The debug monitor software provides a similar user interface to the Analog Devices' Software Simulator. The monitor supports symbolic debugging, full speed execution with or without software breakpoints, single stepping, display/modification of all registers and memory, a disassembler, full display of internal registers and "shadow" registers, logon/logoff commands to record macro command files to disk for later playback, and a DOS shell.

A library of 'C'-callable board drivers for the PC is provided including 'C' and assembly source code, MICROSOFT linkable object modules, and many examples.

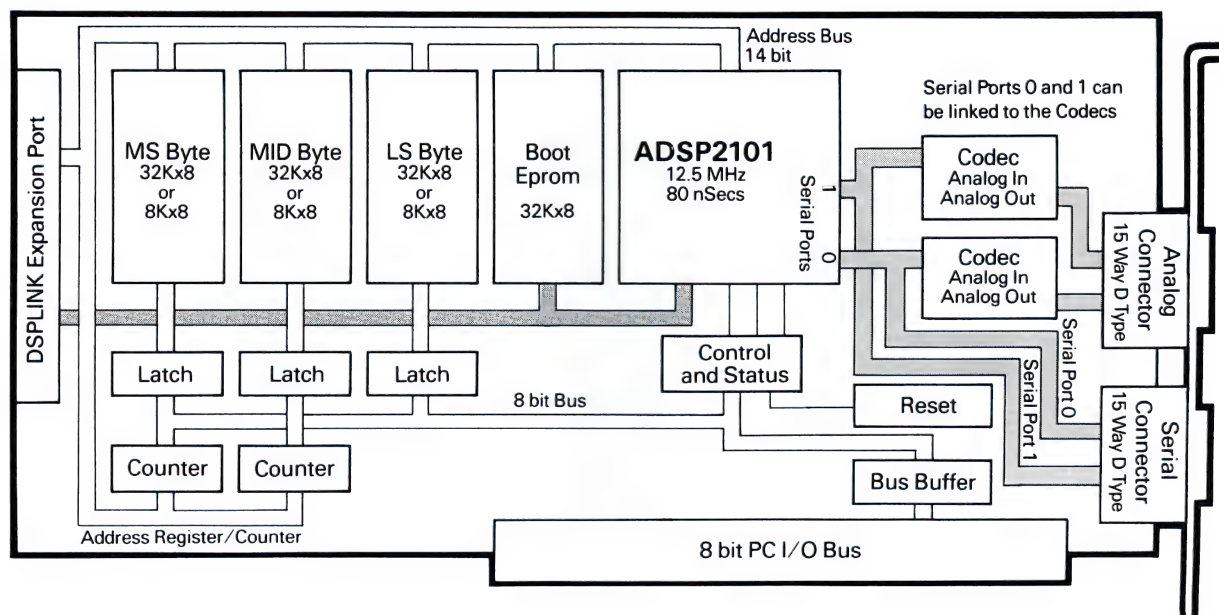
RELATED SOFTWARE PRODUCTS AVAILABLE FROM SPECTRUM

Analog Devices' ADSP-2101 development tools include:

- Assembler/Linker, System Builder, and Simulator
- C Compiler

The System Builder generates a specification of the target hardware environment, which supplies the other development modules with the details they require to assemble, link, and run code. The Assembler/Linker supports the high level syntax of the instruction set and provides a full range of diagnostics.

The Simulator, using the output from the System Builder, assumes the architecture of the user's design, and provides several execution modes, including Emulator mode and Single Step. It has six major display modes and wide variety of utilities and functions.



• Processor

ADSP-2101 running at 12.5 MHz (80ns instruction time).
24-bit instructions and 16-bit data.
16 x 16 multiplier, 40-bit accumulator, & barrel shifter.
2K Words (24-bit) of on chip program memory.
1K Word (16-bit) of on chip data memory.

• Memory

4K Words (24-bit) of program memory expandable to 14K Words.
4K Words (16-bit) of data memory expandable to 12K Words.
All supplied RAM is 35 ns for zero wait-state operation.
Socket for 32K Bytes of EPROM.

• Analog I/O

Dual 19.2 KHz 14-bit codecs (TI TLC32044C).
Two input channels:
Software configurable as single-ended or differential.
Input voltage range: $\pm 3V$, $\pm 1.5V$ (single-ended)
 $\pm 6V$, $\pm 3V$, $\pm 1.5V$ (differential).
Input impedance = 10K ohm.
Includes an 8th order Chebyshev/elliptic 150 Hz anti-aliasing filter with software switchable 3600 hz high pass filter (all cutoff frequencies are software programmable).
Two output channels:
Software configurable as single-ended or differential.
Output voltage range: $\pm 3V$ (single-ended)
 $\pm 6V$ (differential).
Output load: min 600 ohms (single-ended)
min 300 ohms (differential) maximum
capacitance = 100 pf.
Includes reconstruction filter and (sin x)/x correction.

• Serial I/O

Serial interfaces available only when codecs are not in use.
Two full duplex serial ports connected to DB15 style connectors.
6.25 Mbs with internal clock and 12.5 Mbs with external clock.

• Interface to PC Host

8 I/O locations (relocate 8 ways).
Choice of 5 PC interrupts.
Block transfers using auto inc/dec address counters.
16-bit bi-directional communications register with full handshake (polled or interrupt).
8-bit control status register.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus - master.
Up to 5 Mwords/sec transfer rate.
4 of 16 DSP peripheral addresses used.
Standard 50-pin male header ribbon cable connector.
DSP~LINK specifications are available for interfacing application-specific hardware.

• Physical

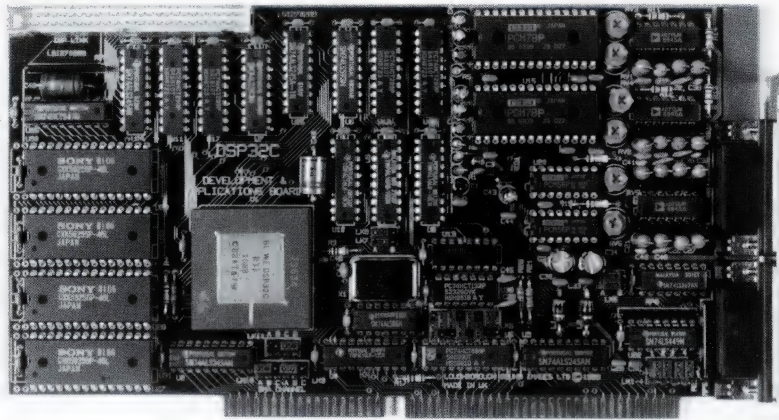
Half-card PC/AT plug-in board.
Dimensions: 8 3/8" L x 4" H x 5/8" D

• Electrical

Power consumption:
+5V @ 1.0A
+12V @ 100 mA
-12V @ 100 mA

DSP32C System Board with Development Support

Part Number: 600-00455



FEATURES

- AT&T DSP32C 80ns floating point DSP.
- **DSP~LINK** System Expansion Interface.
- 40K Words (32-bit) Fast SRAM supplied.
- 136K Word on-board memory capacity (at present).
- Two high-speed 16-bit ADCs and DACs.
- 16 Mbps full duplex serial I/O.
- IBM PC/AT or true compatible plug-in board.
- Monitor software includes single-step, breakpoint, code disassembly and full speed operation.
- Interface function library callable from Microsoft programming languages.

The DSP32C System Board offers high performance, 32-bit floating point signal processing supported by flexible surrounding hardware. Concurrent with other SPECTRUM products, important architectural features of the processor are made available to the user for custom configurations.

The system supports the 80ns instruction cycle, comes with 8 Kwords of zero wait-state static RAM in memory area B and 32 Kwords of two wait-state static RAM in area A. Utilizing the 16-bit data path of the PC/AT bus, the board occupies just 16 locations in the PC/AT's I/O address space. Also supported are: DMA fast transfers, bi-directional interrupts and multiple board installations.

In addition to two on-board, 150KHz analog interfaces, data can also be acquired via the **DSP~LINK** system expansion interface. This 50-pin standardized expansion bus is featured on most SPECTRUM products including multi-channel data acquisition cards. This provides users with the flexibility of tailoring a system to match its analog requirements.

The on-chip serial port is fully buffered and brought out to a DB15 style connector. It supports 8, 16 or 32-bit transfers at clock rates in excess of 16 Mbits per second.

DEVELOPMENT SUPPORT

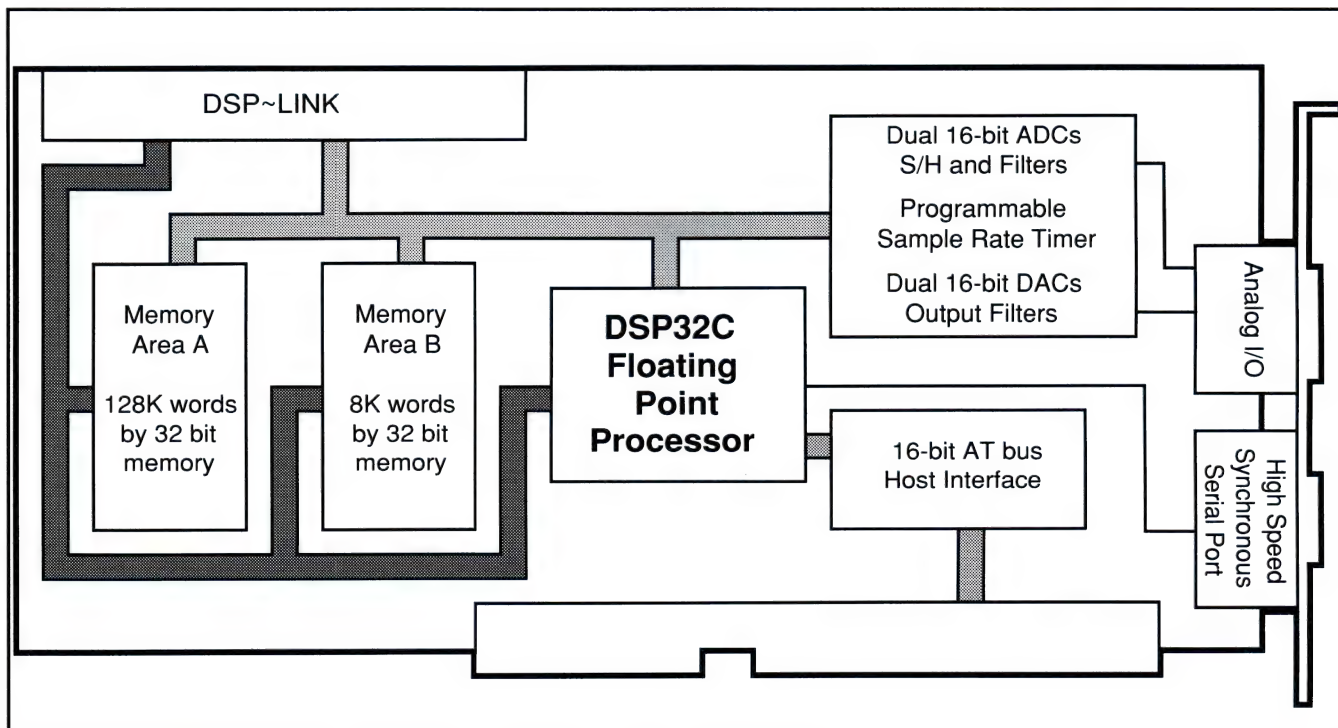
The debug monitor (for VGA & EGA) provided is a graphic intensive, windowed format, featuring pull-down menus and mouse support. Debugging features include single step, breakpoint, disassembly, program loading, data upload/download, register inspection/modification and full speed operation.

Sample programs familiarize the user with DSP32C assembly language and give good examples of how a DSP32C-based system can be used in a PC/AT environment. In addition to these sample programs, AT&T's DSP32C Applications Library is offered, providing object code for many DSP functions including various FFT's and filter functions.

A library of interface functions callable from Microsoft programming languages is provided in two forms. For development purposes, the functions are provided in 'C', allowing the communications techniques to be easily understood and customized if required. For optimization, the functions are also provided in 8086 assembly language.

RELATED SOFTWARE PRODUCTS AVAILABLE FROM SPECTRUM

- DSP32C Assembler/Simulator.
- DSP32C 'C' Language Compiler.
- DSP32C 'C' Callable Application Library.
- **DADISP** Data Analysis software.
- **DISPRO** Digital Filter Design software.
- **Hypersignal-Workstation:**
Integrated workstation for signal processing including data acquisition, filtering, frequency domain analysis, and 3D plots.



- **Processor**

DSP32C running at a 50 MHz clock rate (80ns instruction cycle).
32-bit floating point arithmetic.
Four 40-bit accumulators.
1536 words (32-bit) internal RAM.

- **Memory**

8K x 32 of 25ns RAM in area B.
32K x 32 of 45ns RAM in area A, expandable to 128K x 32.
Memory requiring 2 to 5 wait states can be supplied.

- **Analog Inputs**

Two 16-bit ADCs with sample-and-hold, 153KHz throughput [Burr-Brown PCM78 (5us), Burr-Brown SHC5320 (1.5us)].
Fourth order filtering.
Double-buffered data latching.
Voltage range: $\pm 3V$.
Connections: DB15 style.

- **Analog Outputs**

Two 16-bit DACs [Burr-Brown PCM56 (1.5us)].
Double-buffered data latching.
Fourth order filtering.
Voltage range: $\pm 3V$.
Connections: DB15 style.

- **Analog I/O Clocking Options**

Software initiated conversions.

16-bit timer initiated (minimum sample rate 76Hz) internal/external triggering.

- **Serial I/O**

Synchronous, 16 Mbps.
All signals are buffered.
Clock and Sync can be internal or external.

- **Host Interface**

16-bit PC/AT card format.
Occupies 16 contiguous I/O ports (fully mappable).
Choice of four PC interrupts.
Full DMA implementation.

- **DSP~LINK System Expansion Interface**

16-bit parallel expansion bus
Up to 5 MWords/sec transfer rate.
256 memory-mapped DSP I/O ports available.
Standard 50-pin male ribbon cable connector.
DSP~LINK specifications are available for interfacing application-specific hardware.

- **Physical**

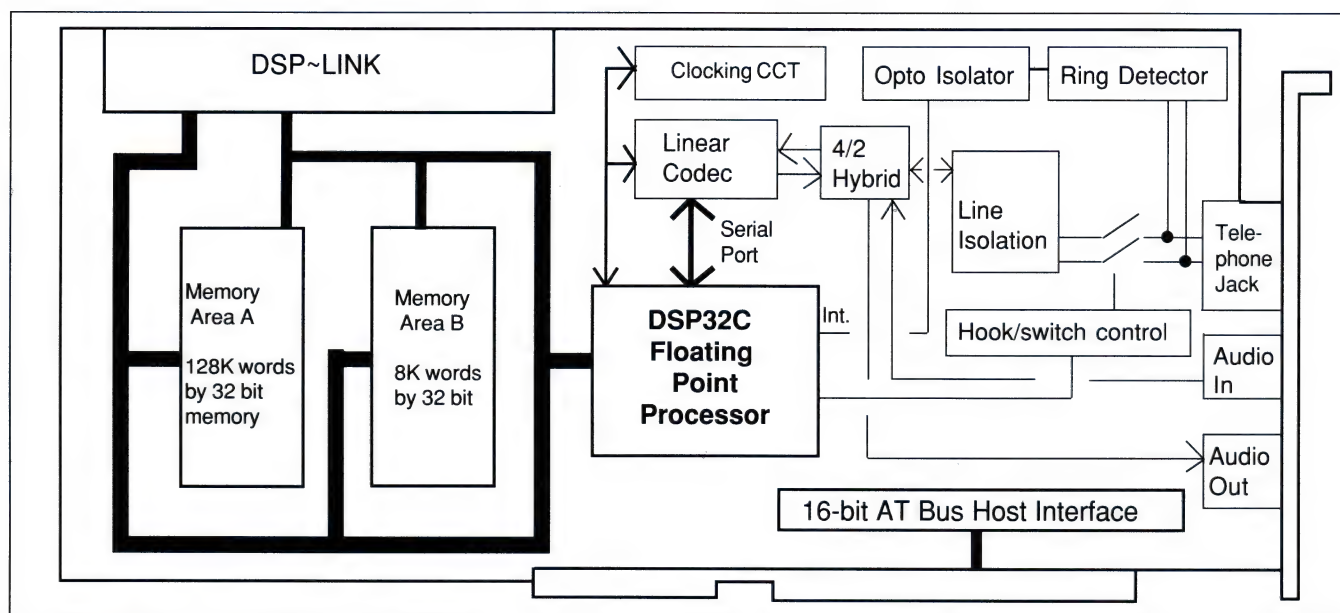
Half-card format PC/AT plug-in board.
Dimensions: 8.75"L x 4.8"H x .5"D.

- **Electrical**

Power consumption: +5V @ 1.2A, +12V @ 150 mA, -12V @ 150 mA.

DSP32C Telephony Board with Development Support

Part Number: 600-00851



FEATURES

- AT&T DSP32C 80ns 32-bit floating point DSP.
- AT&T 7525 Sigma Delta Codec.
- IBM PC/AT PLUG IN TELEPHONY CARD.
- Opto-isolation of Ring Detection Circuitry.
- Transformer Isolation of Line Interface.
- Line level audio input and outputs.
- 40K Words (32-bit) Fast SRAM supplied.
- 136K Word on-board memory capacity (at present).
 - 264K by 32-bits (1st Quarter 1991)
 - 520K by 32-bits (2nd Quarter 1991)
- Telephony software includes DTMF generation, dial pulse generation, DTMF decoding, Voice/Fax & Modem discrimination.
- Monitor software includes single-step, breakpoint, code disassembly and full speed operation.
- Interface function library callable from Microsoft programming languages.

The DSP32C Telephony Board offers high performance 32-bit floating point signal processing supported by a subscriber line interface. The subscriber interface includes ring detectors (opto-isolated), hook switch control, and a transformer coupled line interface.

The system supports the 80ns instruction cycle, comes with 8 Kwords of zero wait-state static RAM in memory area B and 32 Kwords of two wait-state static RAM in area A. Utilizing the 16-bit data path of the PC/AT bus, the board occupies just 16 locations in the PC/AT's I/O address space. Also supported are: DMA fast transfers, bi-directional interrupts and multiple board installations.

The telephony interface supports the standard tip/ring 2 wire
SPECTRUM Signal Processing Inc.

interface. The ring detector will interrupt the DSP32C processor when ringing is detected. The DSP32C has full hookswitch control for seizing and releasing the subscriber line. The linear codec (AT&T 7525 Sigma Delta) passes the data to the DSP32C serially. The DSP32C serial I/O section provides synchronous, double-buffered serial ports for concurrent input and output of serial digital data. Inputs/Outputs can be handled under program control, DMA mode, or interrupt mode.

DEVELOPMENT SUPPORT

The debug monitor provided is a graphic intensive, windowed format, featuring pull-down menus and mouse support. Debugging features include single step, break-point, disassembly, program loading, data upload/download, register inspection/modification and full speed operation.

The telephony software support provides routines to generate or decode DTMF tones, provides for dial pulse outputs and discriminates between voice/fax & modem signals.

Sample programs familiarize the user with DSP32C assembly language and give good examples of how a DSP32C-based system can be used in a PC/AT environment. In addition to these sample programs, AT&T's DSP32C Applications Library is offered, providing object code for many DSP functions including various FFT's and filter functions.

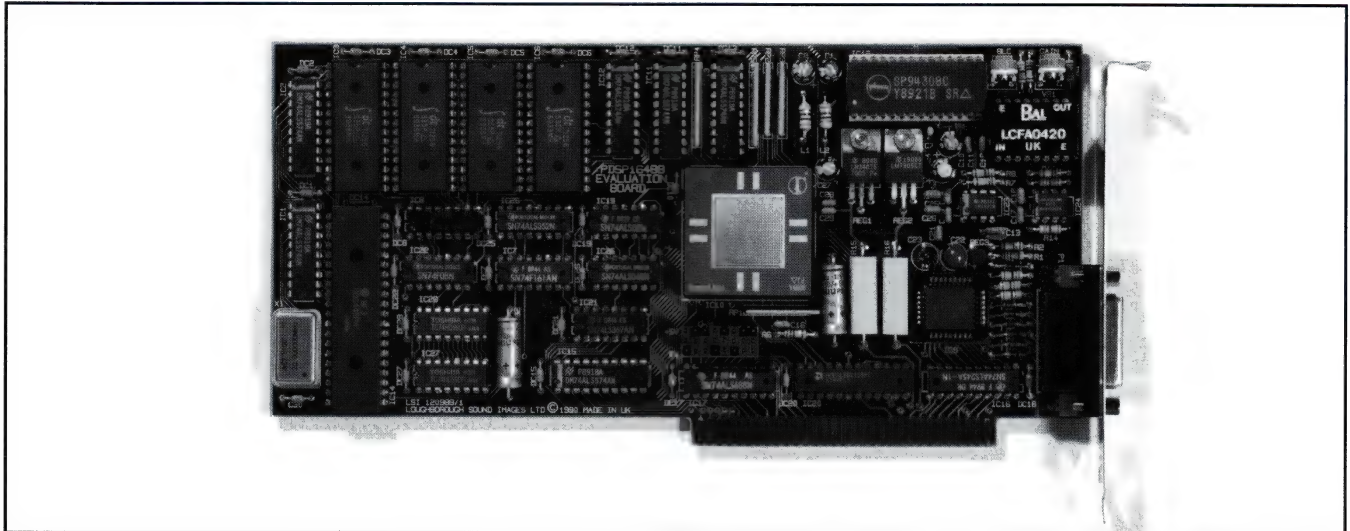
A library of interface functions callable from Microsoft programming languages is provided in two forms. For development purposes, the functions are provided in 'C', allowing the communications techniques to be easily understood and customized if required. For optimization, the functions are also provided in 80286 assembly language.

Eastern US: (508) 366-7355 or 800-323-1842

Western US: 800-663-8986

Canada: (604) 438-7266

with Development Support



FEATURES

- Plessey PDSP-16488 8x8 real-time 2D convolver.
- 256K Bytes memory supporting 512 x 512 frames with 8-bits per pixel.
- High speed 8-bit microprocessor controller.
- Video signals for an RGB monitor.
- Real-time linear, non-linear, and frame "difference" operations.
- Grey-level histograms.
- PC XT/AT plug-in board.
- Menu driven evaluation software.
- 'C' board drivers.

The PDSP-16488 Imaging/Graphics Board is a PC plug-in card consisting of a video digitization section, field and frame stores, a Plessey PDSP-16488 image convolver, and an output display system. A high speed 8-bit microprocessor subsystem controls the operation of the above components and provides communications with the host PC.

The board facilitates real-time linear operations on a picture using the image convolver and non-linear operations using color look-up tables. Operations can also be carried out which highlight the changes in a picture between two frames, including spatial and field-to-field change effects.

VIDEO DIGITIZATION

Two software selectable video inputs for standard RS170 or PAL video signals are supported. Each input is terminated and buffered before being band limited. Synchronization is achieved by phase locking the video pixel clock to an incoming line frequency. Sync separation is performed to provide composite and vertical sync, and odd/even field outputs. Full 8-bit digitization is performed at a 10 MHz sampling rate.

FRAME/FIELD STORAGE

Since interlaced pictures must have the interlacing removed before convolution, field stores for odd and even fields are fed simultaneously to the convolver. Each field of 512x512 frame requires 128K Bytes of storage assuming 8-bits per pixel. A further single frame store is used at the output of the convolver for intermediate results.

CONTROL MICROPROCESSOR

The control microprocessor acts as an interface between the commands issued by the host PC and the on-board hardware. Communications with the PC occurs during active display and RAM look-up table and convolver coefficient updating is performed during field blanking.

DEVELOPMENT SOFTWARE

A menu-driven software package is included to control the operation of the convolver and the output look-up table.

The main screen displays the 8 x 8 convolution matrix both numerically and in a grey-scale representation. The gain of the convolver is controlled via a "slider". Changes made on the PC screen are instantly reflected in the operation of the convolver. Sets of control parameters can be saved on disc and recalled at any time. Functions to 'freeze' a field and perform grey level histograms are also provided.

In addition, a library of 'C'-callable board drivers for the PC is provided including 'C' and assembler source code, MICRO-SOFT linkable object modules, and many examples.

Processor Boards

Selection Guide

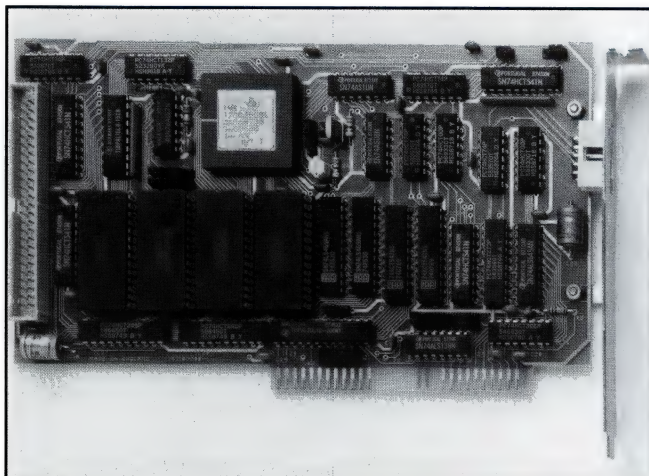
Product	TMS320C25 Data Acquisition Proc. Brd.	TMS320C25 Processor Board	TMS320C30 Processor Board	DSP56001 Processor Board	Dual DSP56001 Processor Brd.	DSP32C Processor Board
Part Number	600-00626	600-00266	600-01011	600-00211	600-00752	600-00662
Host Bus	IBM AT/XT	IBM AT/XT	IBM AT	IBM AT/XT	IBM AT	IBM AT ⁽²⁾
Processor Instruction Cycle Precision Accumulators Internal Memory	100ns ⁽¹⁾ 16-bit integer 1 x 32-bit 544 Words	100ns ⁽¹⁾ 16-bit integer 1 x 32-bit 544 Words	60ns 32-bit floating pt. 8 x 40-bit 2048 Words 64 Word CACHE	100ns ⁽⁶⁾ 24-bit integer 2 x 56-bit 1024 Words	74ns ⁽³⁾ 24-bit Integer 2 x 56-bit 1024 Words	80ns 32-bit floating pt. 4 x 40-bit 1536 Words
On-Board Memory Standard Maximum	128K x 16 Local 256K x 16 Buffer 128K x 16 Local 2M x 16 Buffer	16K x 16 64K x 16	64K x 32 64K x 32 ⁽⁷⁾ 192K x 32	48K x 24 192K x 24	66K x 24 4K x 16 ⁽⁷⁾ 66k x 24 4K x 16 ⁽⁷⁾	40K x 32 136K x 32
Serial I/O	1 Synch (5 Mbps)	1 Synch (5 Mbps)	2 Synch (8.3 Mbps)	1 Synch (5 Mbps)	2 Synch ⁽⁴⁾ (RS-422)	1 Synch (16 Mbps)
Parallel I/O Interface	DSP~LINK	DSP~LINK	DSP~LINK	DSP~LINK	Motorola ADS ⁽⁵⁾	DSP~LINK
Application Software: Real-Time O.S. C Compiler	TI or LSI	TI or LSI	SPOX™ TI	Motorola	Motorola	AT&T

Footnotes:

- (1) 80ns with TMS320C25 - 50 MHz (P/N 600-00653)
- (2) Full DMA implementation
- (3) Uses two Motorola DSP56001 processors running at 27 MHz
- (4) Also can be configured as SLD to communicate with Intel ISDN chip set
- (5) DSP~LINK Interface Module Available
- (6) 74ns with DSP56001 - 27 MHz (P/N 600-01065)
- (7) Memory is dual ported between the DSP and PC Host.

TMS320C25 Processor Board with Development Support

Part Number: 600-00266



Occupying only 8 I/O locations in the PC's address space (relocatable to 8 places), users may configure up to 8 processor boards into one PC. There are on-board address counters for efficient block transfer operations. The PC has direct access to all external RAM, and can read and write both program and data memory while the processor is held.

Data can be acquired via the **DSP~LINK** system expansion interface. This 50-pin standardized expansion bus is featured on most SPECTRUM products including multi-channel data acquisition cards, providing users with the flexibility of tailoring a system to match their analog and digital I/O requirements.

SPECTRUM provides a similar board with on-board analog I/O called the "TMS320C25 System Board". Please refer to the appropriate data sheet for information on this product.

FEATURES

- TMS320C25 16-bit 100ns processor.
- 64 Kwords of on-board memory capacity.
- **DSP~LINK** System Expansion Interface.
- Global memory capability via DSP~LINK.
- 5 Mbps full-duplex serial I/O.
- IBM PC/XT/AT or true compatible plug-in board.
- Monitor software including single step, breakpoint and full-speed operation.
- 'C' board drivers.

The TMS320C25 runs at full speed (100ns instruction cycle) and comes with 16 Kwords of 45ns RAM for zero wait-state operation. The 64 Kwords of merged memory can contain any mix of data and programs.

DEVELOPMENT SUPPORT

A complete debug monitor is provided for software development and debugging. Monitor features include single-step, breakpoint, disassembly, program loading, data upload/download, register inspection/modification, or full-speed operation.

Sample programs familiarize the user with program development and give good examples of how the processor board can be used in the PC environment. These programs include a 128 point FFT, a real-time FIR filter, and a data-logger.

A library of 'C'- callable board drivers for the PC is provided including 'C' and assembly source code, MICROSOFT linkable object modules, and many examples.

• Processor

TMS320C25 running at 40 (or 50) MHz clock rate.
16-bit processing including 16 x 16 hardware multiplier, and 32-bit ALU.
544 words (16-bit) of internal RAM.
8 auxiliary registers for address pointers & loop counters.
Internal interval timer.

• Memory

System comes with 16K x 16 45ns RAM.
Supports up to 64K x 16 RAM (configurable as any mix of program or data RAM).
PC can access TMS320C25 memory while TMS320C25 is running.

• PC Interface

8 I/O locations (relocate 8 ways).
Choice of 5 PC interrupts.
Block transfers using auto inc/dec address counters.
16-bit bi-directional communications register with full handshake (polled or interrupt).
8-bit control/status register.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus - master.
Up to 5 Mwords/sec transfer rate.
14 DSP I/O ports available (2-15).
2 DSP interrupts.
Standard 50-pin male header ribbon cable connector.
DSP~LINK specifications are available for interfacing application-specific hardware.

• Serial Interface

5 Mbps, full duplex, internal external clock and sync, continuous or burst data, 8 or 16-bit data.
Buffered TMS320C25 serial port signals.
Multi-processor capability.
Standard 10-pin header connector (on PC backplate).

• Physical

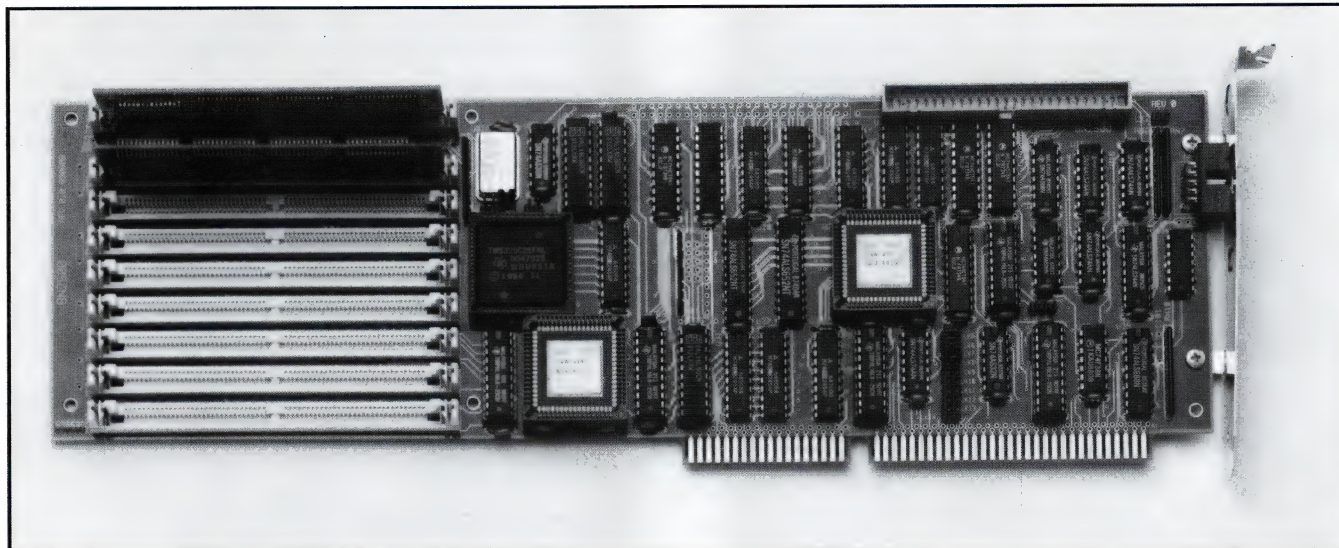
IBM PC/XT/AT "short" card format.
Dimensions: 7" L x 4.5" H x .5" D.

• Electrical

Power consumption: 5V @ 1.5A max.

TMS320C25 Data Acquisition Processor with Development Support

Part Number: 600-00626



FEATURES

- TMS320C25 16-bit 100ns DSP processor.
- **DSP~LINK** System Expansion Interface.
- 64 Kwords Data Memory.
- 64 Kwords Program Memory.
- 2 Mword on-board Data Buffer Capacity (future up to 16 Mword).
- High speed data Buffer Management Unit (BMU) with **BMU~LINK** interface.
- Global memory capability via **DSP~LINK**.
- 5 Mbps full-duplex serial I/O.
- IBM PC/XT/AT 8/16-bit bus interface.
- Monitor software includes single-step, breakpoint, code disassembly and full speed operation.
- 'C' board drivers.

The TMS320C25 Data Acquisition Processor Board is designed specifically for applications which must acquire and process large amounts of data. The key features of this system are the Buffer Management Unit (BMU) and large data buffer (up to 2 Mwords) which effectively extend the addressing and processing capability of the Digital Signal Processor. The functions performed by the BMU include the following:

- 24-bit buffer address generation (up to 16 Mwords)
- Circular buffer management
- Multiple data channel support
- Data Compare functions
- Sample counter

The BMU handles data manipulation functions, leaving the DSP free to accomplish signal processing tasks such as filtering, modulation, and transforms. As a result, the effective throughput of the processor is substantially increased over other DSP-based data acquisition and analysis systems.

The board occupies 8 consecutive I/O locations in the PC and the base location is mappable, allowing installation of up to 8 boards in the same PC. The PC can execute block transfers to and from both program and data memory using autoincrement/decrement addressing. Control and operation of the buffer management unit are accessed through two ports in the C25 I/O space.

The TMS320C25 Data Acquisition Processor Board is compatible with both 8 and 16 bit PC/XT/AT busses and will support both byte and word transfers for optimum performance. A 16-bit bidirectional mailbox register

allows message passing between the PC and the C25, useful for passing control and status information "on the fly". Access to the mailbox by either the PC or the C25 can be configured to generate an interrupt to the other processor.

Traditional PC-based data acquisition systems suffer two major limitations: the memory limitations of DOS; and the transfer speed of the PC bus. The TMS320C25 Data Acquisition Processor Board eliminates these two problems because its memory buffer is independent of the PC's memory address space. Data can be acquired in real time without size or speed constraints imposed by the PC. Transfer to PC memory and/or disk can be made after acquisition and/or processing. Using the flexibility of the BMU, the buffer can be partitioned into smaller areas for fast access data for PC display, vector operations, table storage and window functions, etc. For image processing applications the data can be scanned by rows or columns using the increment function on the BMU hardware.

Analog data can be acquired via the DSP~LINK system expansion interface. This 50-pin standardized expansion bus is featured on most SPECTRUM products, including a selection of multi-channel data acquisition cards, providing the flexibility of tailoring a system to match its analog and digital I/O requirements.

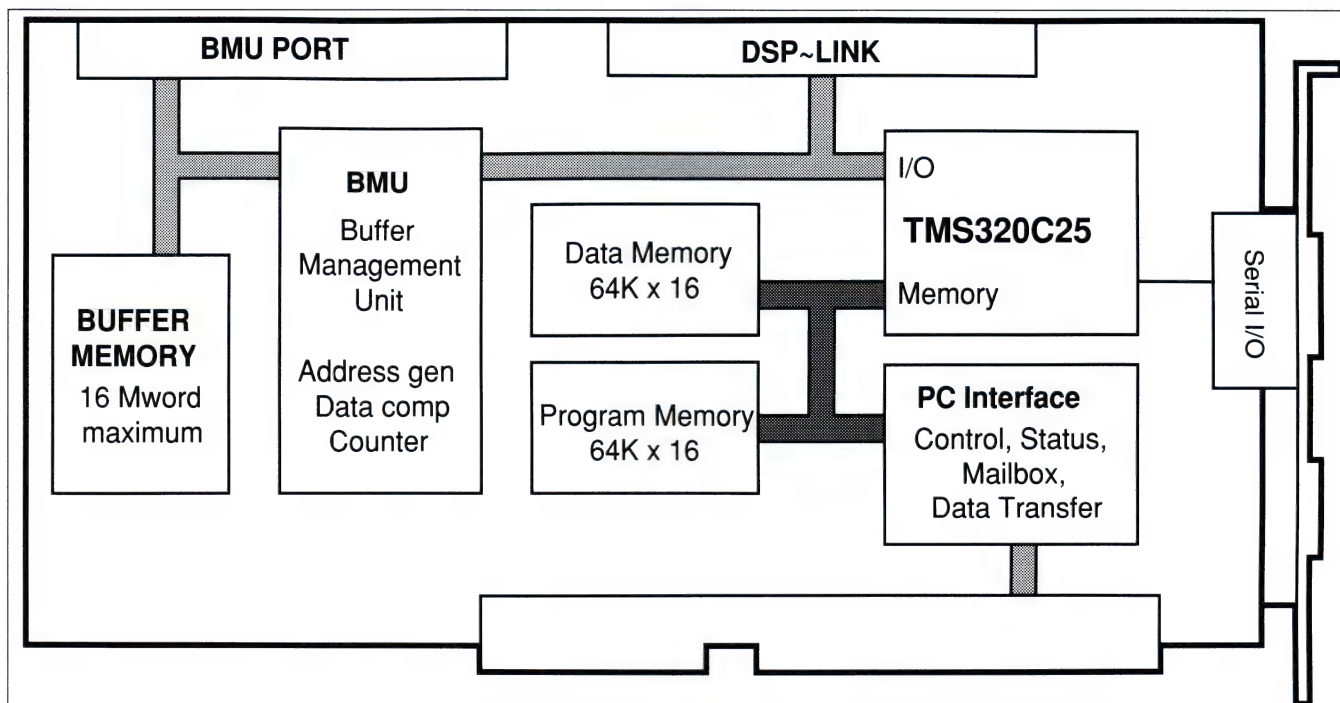
For high speed data acquisition, which cannot be supported by the **DSP~LINK/TMS320C25** Processor interface, the "**BMU~LINK**" interface is provided to dump data directly to buffer memory under BMU control. This interface removes the TMS320C25 from the data path allowing transfer rates dependent only on the buffer memory access time. This feature is completely software selectable.

DEVELOPMENT SUPPORT

A complete debug monitor is provided for software development and debugging. Features include single step, breakpoint, disassembly, program and data transfers, register status and modification, as well as full speed program execution.

Sample programs familiarize the user with program development and give numerous examples of how the system can be effectively used. These routines include a 128-point FFT, a real time FIR filter, and a data logger. Source code is included as part of the documentation.

A library of C-callable board drivers for the PC are provided including C and assembly source code, Microsoft linkable object modules and many examples.



• Processor

TMS320C25 running at a 40 MHz clock rate (100ns instruction cycle).
16-bit data path with 16 x 16 multiplier, 32-bit ALU.
544 words (16-bit) internal data RAM.
8 Auxiliary registers, internal interval timer.

• Memory

Standard system configuration:

Program memory	32 Kword 0 wait-state
	32 Kword 1 wait-state
Data memory	64 Kword 1 wait-state
Buffer memory	256 Kword 1 wait-state
Program and data memory can be factory upgraded in 32K Word blocks.	

Buffer memory can be incremented in 256K blocks up to 2M words.

Future memory components will allow full 16Mwords on board.

• Buffer Management Functions

Buffer memory address generator:

Autoincrement/decrement in steps of 0 to 32,384 facilitating multiple channel operation.
Autoincrement/decrement enabled for read, write, or both.
Circular buffer can be implemented between any two addresses in 16M Word address space.

Data compare function:

Data read/written to buffer is compared to stored value or to previous value.
Detects trigger at specified level, pos./neg. slope.
Allows maxima/minima detect.
Result of data compare is used to enable counter.

Counter function:

Counter can be enabled by results of compare function.
Range 0 to 16M counts.
Allows implementation of pre-trigger, post-trigger or any intermediate trigger point for data capture.
External enable available for external triggering.

• Host Interface

PC/XT/AT compatible.
16-bit or 8-bit data bus for optimum data transfer.
8 consecutive I/O locations (mappable 8 ways).
Choice of 11 PC interrupts.
Block transfers using auto increment/decrement.
16-bit bidirectional mailbox with full handshake.
8-bit control/status register.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus, 12 DSP I/O ports available.
Up to 5 Mwords/sec transfer rate.
Standard 50-pin male ribbon cable connector.
DSP~LINK specifications are available for interfacing application-specific hardware.

• BMU~LINK System Expansion Interface

16-bit parallel expansion bus.
Direct transfer to buffer memory.
Maximum sustainable transfer rate
5MHz (40MHz processor)
6.25 MHz (50MHz processor)
Standard 50-pin male ribbon cable connector.
BMU~LINK specifications are available for interfacing application-specific hardware.

• Serial Interface

5 Mbps full duplex, internal/external clock and synch, continuous or burst data, 8 or 16-bit length.
Buffered TMS320C25 serial port signals.
Multi-processor capability.
Standard 10-pin header connection (PC backplate).

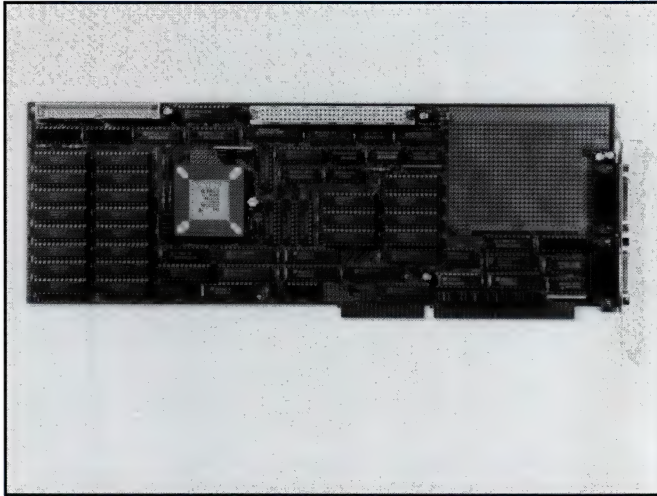
• Physical

Full length PC/AT plug-in board.
Dimensions: 13.375" x 4.15" x 1.5"
Occupies 2 PC slots, with or without DSP~LINK peripheral half card.

• Electrical

Power consumption: Maximum 2A @ 5V, Typical 1A @ 5V.

with Development Support



FEATURES

- 33 MHz TMS320C30 Digital Signal Processor
- DSP-LINK System Expansion Interface.
- 128 Kwords of Fast SRAM, expandable to 192 Kwords.
- Memory expansion connector for 16 Mword Memory Daughter Board.
- Large wire wrap prototyping area.
- Two 8.3 Mbps general purpose serial ports.
- Window based monitor debugger.
- Optional SPOX™ DSP Operating System and Application Programming Interface.
- High level language interface function library

The TMS320C30 Processor Board is an IBM PC plug-in board designed to support both hardware and software development for OEM applications using Texas Instruments' 33 MHz TMS320C30 digital signal processor.

The board is supplied with 64 Kwords of 0 wait-state local SRAM and 64

Kwords of 1 wait-state SRAM dual-ported to the IBM PC. The local memory is expandable by an additional 64 Kwords for a total of 128 kwords. The TMS320C30's entire 16 Mword address space is accessible using the C30 Memory Expansion Daughter Board.

A 55 cm² prototyping area is provided for users to wire-wrap or solder custom analog and digital I/O circuits. This area is a 0.1" matrix of plated-through holes with a ground plane on the inner layers. Two rows of holes are dedicated to +5V and GND with +12V and -12V also available. In addition, the secondary address and data lines of the TMS320C30 along with interrupt, timer, and reset signals are brought out from the processor to the prototyping area. For convenience, an uncommitted 15 pin D-type connector is provided on the endplate.

I/O mapped, the board occupies 16 locations on the AT Bus with facilities for bi-directional interrupts and multiple board installations. The board memory is addressed by the PC using a 24-bit up/down counter and a 32-bit bi-directional register allows blocks of data to be transferred at high speed.

Data can be acquired via the DSP~LINK system expansion interface. This 50-pin standardized expansion bus, available on all SPECTRUM products, allows users to configure a system to match their specific analog and/or digital I/O requirements.

DEVELOPMENT SUPPORT

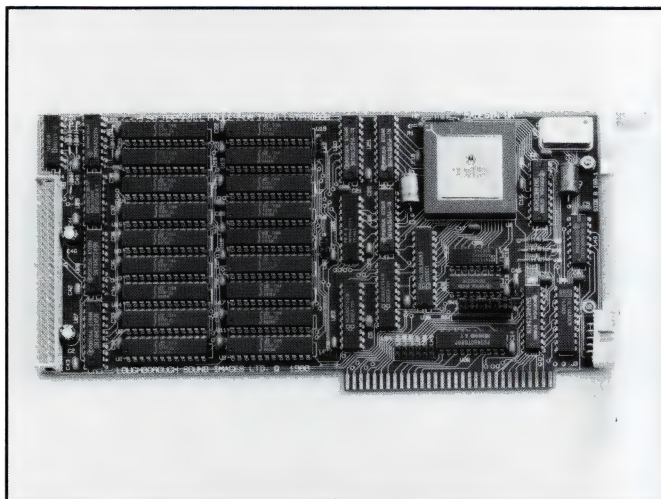
The debug monitor (for EGA and VGA) provided is a graphic intensive, windowed format, featuring pull-down menus and mouse support. Debugging features include single step, breakpoint, disassembly, program and data transfers, register status and modification, as well as full speed execution. Sample programs familiarize the user with TMS320C30 assembly language and give good examples of how to use the board.

A library of interface functions callable from Microsoft programming languages is also provided to allow easy integration of the DSP application with the PC/AT user interface. In addition, the SPOX™ operating system is available which provides standard I/O support for C programs and a library of standard DSP system functions which free the user from writing low level DSP code.

- **Processor**
Texas Instruments TMS320C30 running at 33 MHz
32-bit floating point arithmetic.
64 x 32 instruction cache and eight 40-bit accumulators.
Two 1K x 32 dual access RAM.
One 4K x 32 dual access ROM.
Two 32-bit general purpose timers.
- **Memory**
C30 Local: 64K x 32, 0 wait-state (25 ns), expandable to 128K x 32.
Dual-Ported to PC: 64K x 32, 1 wait-state (35 ns)
Off-Board: memory expansion connector facilitates expansion to full C30 capacity of 16 Mwords.
- **Prototyping Area**
55 cm², 0.1" matrix of plated through holes.
Complete access to TMS320C30's secondary bus.
+5V and GND along with decoupled +/-12V available.
Uncommitted DB15 connector is available.
- **Serial I/O**
Two synchronous 8.3 Mbps serial ports.
Fully buffered for 8, 16, 24, or 32 bit transfers.
Software configurable.

Standard DB15 connector.

- **Host Interface**
16-bit PC/AT format.
Occupies 16 contiguous I/O ports (fully mappable).
Choice of six PC interrupts.
Transfer rates: 1.2 Mbytes/sec, PC to processor board
800 Kbytes/sec, processor board to PC.
- **DSP~LINK Expansion Interface**
16-bit parallel expansion bus.
5 Mwords/sec maximum bus transfer rate.
8192 memory mapped I/O ports available.
Standard 50-pin male header ribbon connector.
DSP~LINK specifications are available for interfacing to custom hardware.
- **Physical**
Full length PC/AT plug-in board.
Dimensions: 13-3/8"L x 4-5/8"H x 5/8"D.
- **Electrical**
Maximum power consumption:
5V at 2.0A, 12V at 150mA, -12V at 150mA



FEATURES

- Motorola 56001 24-bit 100ns processor.
- **DSP~LINK** System Expansion Interface.
- 192 Kwords of on-board memory capacity.
- IBM-PC/XT/AT or true compatible plug-in board.
- Monitor software including single step, breakpoint and full-speed operation.
- 'C' Board drivers.

The system runs with a 100ns instruction cycle and comes with 48 Kwords of 35ns static RAM for zero wait-state operation. Host access to system memory, peripherals and registers is achieved using the 56001's specialized host interface. The interface appears to the host (PC) as a block of sixteen locations in its I/O address space.

Data can be acquired via the **DSP~LINK** system expansion interface. This 50-pin standardized expansion bus is featured on all SPECTRUM products including multi-channel data acquisition cards, providing users with the flexibility of tailoring a system to match its analog and digital I/O requirements.

A single 5 Mbs synchronous serial port is provided. It is fully buffered and brought out to a 10-pin connector at the rear of the PC.

SPECTRUM provides a similar board with analog I/O called the "DSP56001 System Board". Please refer to the appropriate data sheet for information on this product.

DEVELOPMENT SUPPORT

Debug monitor software is provided in two forms. A simple, command-driven version and a window-based menu-driven version. Its features include memory-register examination and modification, program downloading, disassembly, single step, and multiple event-counting breakpoints.

Sample programs familiarize the user with 56001 Assembly language and give good examples of how this board can be used in a PC environment. The sample programs include a 1024-point FFT, a FIR filter and a data logger. Source code is included as part of the system documentation.

A library of 'C'- callable board drivers for the PC is provided including 'C' and assembly source code, Microsoft linkable object modules, and many examples.

• Processor

56001 at 20 MHz clock rate (100ns instruction cycle).
24-bit processing including 24 x 24 hardware multiplier and two 56-bit accumulators.
512 words (24-bit) internal data RAM.
512 words (24-bit) internal program RAM.
Four (4) data busses.
Internal ROM contains μ law/A-law to linear and sine tables.

• Memory

System comes with 48K x 24 of 35ns RAM (16K x 24 in each of PGM, X, and Y).
Supports up to 192K x 24 of on-board memory (64K x 24 in each of PGM, X, and Y).
Slower RAM or EPROMs can be used by programming software selectable wait-states.

• Serial I/O

Synchronous (SSI) 5MHz: 10-pin connector on end plate.

• Interface to PC Host

56001 host interface mapped into a block of 16 I/O locations in the PC.
On-chip integration of this interface provides low overhead access to registers, memories and peripherals.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus - master.
Up to 5 MWords/sec transfer rate.
63 DSP I/O ports available (Y: FF01-FFFF).
2 DSP interrupts.
Standard 50-pin male header ribbon cable connector.
DSP~LINK specifications are available for interfacing application-specific hardware.

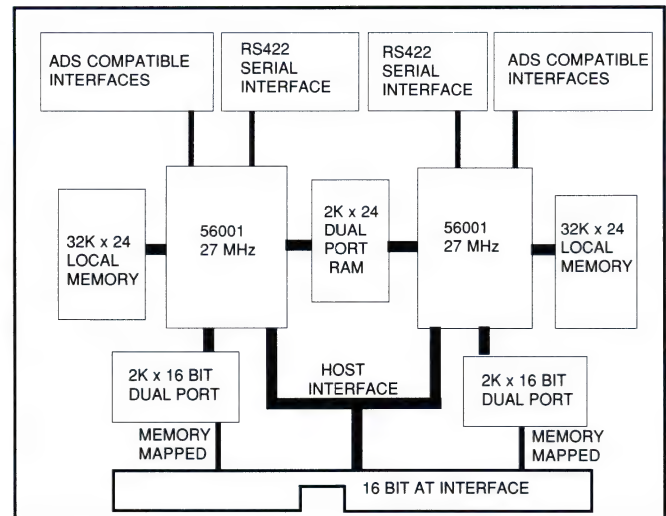
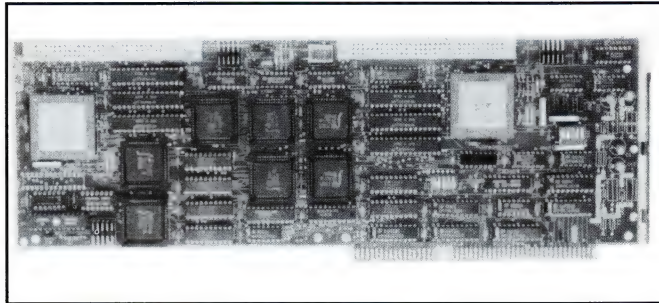
• Physical

Full-length IBM-PC plug-in card.
Dimensions: 13-3/8" L x 4-1/2" H x 5/8" D.

• Electrical

Power consumption: 5V @ 2A max.

with Development Support



FEATURES

- 27 MIPS with two 27 MHz Motorola DSP56001 24-bit processors.
- 32k x 24-bits zero-wait state local memory for each processor.
- 2k x 16-bits zero-wait state dual port RAM between host and each processor.
- 2k x 24-bits zero-wait state dual port RAM between processors.
- Two Motorola ADS compatible peripheral expansion sockets.
- RS422 Intel SLD ISDN serial interface each processor.
- IBM-AT or compatible plug-in board.
- Monitor software including bootstrap, upload, download, single step and break point facilities.
- Optional peripherals include a stereo analog interface and an Adaptive Fir Filter.

This Dual Processor DSP Board is based on two Motorola DSP56001's. Each processor has a 74 ns instruction cycle, which combine to provide 27 MIPS of processing power.

Local memory for each processor consists of 32K x 24 bits of 30ns static RAM for zero-wait state operation. Host access to each processor is achieved using either the DSP56001's host/DMA interface or 2K x 16-bits of 35ns dual-port RAM for real time transfers. Interprocessor communication is achieved using 2K x 24-bits of 35ns dual-port RAM.

Every pin of each DSP56001 and +/-5V and +/-12V is brought out to a peripheral expansion socket that is compatible with the Motorola ADS DSP56001 Development System. So far, 2 peripheral cards have been developed for the system, one a programmable 16-bit stereo analog interface, the other a 2048 tap Adaptive FIR Filter Module that can be used as an acoustic echo canceller.

The board has a synchronous serial interface option which can be ordered to be either a high speed RS422 interface for interboard communication or an SLD interface for communication with the Intel ISDN chip set (RS422 Standard).

DEVELOPMENT SUPPORT

Debug monitor software is provided. Its features include a memory-register examination and modification, program downloading and disassembly.

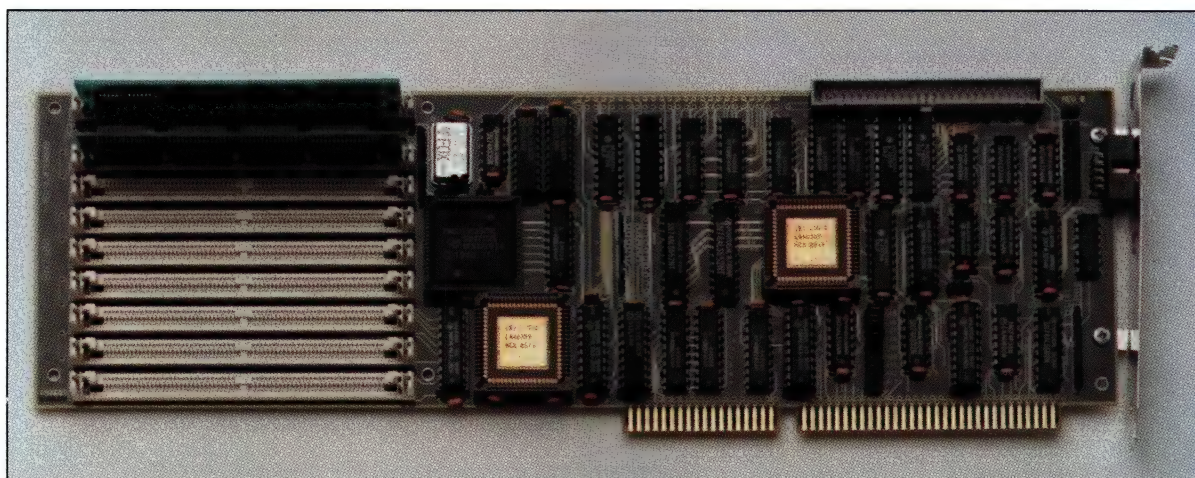
Sample programs familiarize the user with the dual architecture DSP56001s and give examples of how this board can be used in a PC environment. Source code is included as part of the system documentation.

A library of 'C' board drivers for the PC is provided which can be easily integrated into the user's own PC interface code using standard 'C' calling conventions.

Motorola's DSP56000CLASx support software including relocatable Assembler, Linker/Librarian and Simulator is available separately from SPECTRUM. The Motorola 'C' compiler for the DSP56001 is also available from SPECTRUM.

Selecting a DSP chip is no simple chore

There are numerous things to consider to best match a digital signal processor to an application



Proven performers include the Texas Instruments TMS320C25 DSP chip, used here in a data acquisition processor board from Spectrum Signal Processing.

BY WARREN B. COPE
Spectrum Signal Processing
Vancouver, BC, Canada

Though designing a DSP-based system has never been a trivial task, choosing chips for such a system is becoming even more complex. An abundance of DSP engines is available from a variety of manufacturers. Word lengths reach 32 bits, and some chips have superb floating-point capability.

But selecting these chips goes beyond merely comparing such features. The performance available from most DSP-based systems depends largely on how the main processor performs with its peripheral

environments. A system design built on a particular processor selected for seemingly sound reasons may be flawed if the system interface or development network used to create the design is inadequate.

Taking a broad view of the project and reviewing every variable as early as possible is important. Designers must resist the temptation to select a DSP chip without having full knowledge of the compilers, debuggers, and other tools either available or soon to be released.

Many designers may also rely on the kind of key criteria they used in making decisions about microprocessor-based designs. There are some significant differences in the two types of designs. For example,

the tools for DSP designs simply may not yet be available and proven.

An orderly approach

With so many facets of the design to consider, a clear, orderly methodology is required to avoid hasty or incomplete decisions and prevent the process from becoming needlessly complicated. To make the correct chip selection and complete the project on time, the system design team must thoroughly consider three broad categories of design criteria:

- The relationship of the DSP system to its application, including an overall cost and the market window for the project or system.
- The availability of hardware and software tools to create a develop-

ment environment that can succeed.

- The memory, data rate, ergonomic factors, and other interface issues that pertain to the system.

DSP engine selection

Should the design rely on a proven DSP chip or use a newer processor? Proven performers include the Texas Instruments TMS320C25 and its predecessors. Newer processors, using different architectures, include the Motorola 56001 and 96002 and the Texas Instrument TMS320C30, as well as processors from AT&T, Analog Devices, Oki Semiconductor, and Siemens.

DSP processors come in different word sizes—16-, 24-, and 32-bit—and are designed specifically for fixed-point or floating-point requirements. The differences are significant. The newer, 32-bit floating-point processors typically have 40-bit accumulation, which is needed to support multiplication bit requirements. The *table* on this page offers a quick look at the type of processor that is usually most appropriate for various DSP-based designs. The list is intended only as a general starting point.

By examining the application, the designer can also estimate memory requirements and approximate complexity—a measure of the operations per second required to perform the number of math features and table searches. The user must investigate how much data memory is required, as well as the expected size of program memory.

Because the leading DSP engines also provide internal memory, the user must explore whether the processor's memory is sufficient to handle the load. Furthermore, from both an ease of function and accounting angle, using a Harvard memory architecture (which has separate data and program memories) can significantly affect the circuit board layout, increasing final system cost. Such increased costs may not be warranted in many designs.

Analog interface requirements vary with each application. The key factors are noise, dynamic range, and throughput. Module-to-module interconnects also play a vital role in reviewing overall system throughput. In more and more DSP-based

designs, non-Harvard architectures may be more cost-effective.

A designer should also rate the board layout for its simplicity and estimate its potential power once the program code is in place. For example, the designer should understand whether the target application supports slower EPROM accessing and

faster RAM accessing. The designer should also determine whether the processor can load slow EPROM into rapid RAM prior to execution, as well as compare net outcome of the download.

The user also needs to understand the approximate complexity of the ultimate program. Since the inputs to

Basic Processor Criteria by Application

The following table summarizes some typical DSP applications and lists the associative applicability for the various DSP parameters.

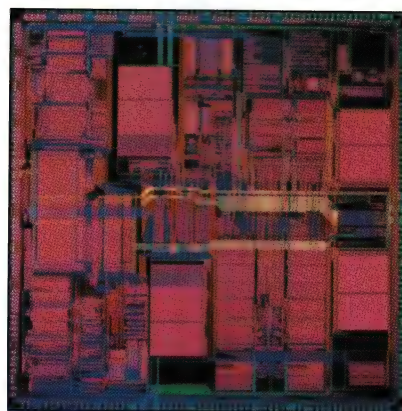
An entry states the appropriate bit and math requirements for typical applications. This does not mean that another processor configuration is inappropriate. It simply states from experience effective minimal solutions for that application.

APPLICATION	Appropriate Data Bits	Fixed or Floating Point
ELECTRONIC DATA PROCESSING		
Mass memory		
Disk controllers	16	Fixed
Servo controllers	16	Fixed
Workstations		
Graphics	16	Float
Translations	16	Float
Rotations	32	Float
Shading	16	Fixed
Perspective scaling	32	Float
Inversion	16	Fixed
Multiplication	32	Float
Numeric accelerators	32	Float
Array processing	32	Float
INDUSTRIAL		
Robotics		
Image processing (Pattern matching, recognition, alignment)	32	Float
Process control	16	Fixed
Real-time simulators	32	Float
Instrumentation (Oscillosopes, FFT, analysis, signal generators)	32	Float
TELECOMMUNICATIONS		
PBX		
Tone detection	16	Fixed
Tone generation	16	Fixed
DTMF	16	Fixed
Switches		
Tone detection/generation	16	Fixed
Line testing	16	Fixed
Modems/Fax		
Echo cancellation	16	Fixed
Filtering	16	Fixed
Error correction and detection	16	Fixed
Modulation/demodulation	16	Fixed
Transmission		
Multi-pulse	16	Fixed
LPC	16	Fixed
ADPCM	16	Fixed
Encryption	16	Fixed
Adaptive equalization	16	Fixed
Data compression	16	Fixed
Data encryption	16	Fixed
Data scrambling	16	Fixed
Tone generation	16	Fixed
μ-law/A-law conversions	16	Fixed

most DSP applications are externally imposed, a DSP system must be able to execute its code at a speed determined by the input, or it does not work at all.

This can be checked by loosely coding within the target processor the significant portions of the application algorithm. The result is a rough estimate of the number of cycles required. Then, by comparing this result with the total number of cycles the processor can deliver, the designer may eliminate the processor from consideration, if it clearly cannot do the job.

After the DSP engine's suitability to the application has been determined, the designer should consider how much existing software supports the processor. For many designs, the software includes C compilers, debuggers, monitors, emulators, and assembler/linkers. Packages that include computer-aided software engineering tools are also arriving from a variety of vendors. Unfortunately, such tools may be in short supply for the more advanced, technically superior DSP chips. This unavailability may make develop-



The Motorola 96002 DSP chip has 750,000 transistors, including about 12 Kbytes of RAM and ROM.

ment impossible, considering the market window.

For the established older chips, such as the original TMS320 devices from TI, tools are pretty well proven now. That proven status may be decisive in making a selection.

Development boards are also becoming increasingly valuable in system development and prototyping. They speed application development and add significant reliability to the process. An increasing number of

boards supporting a wide variety of development options are coming to market from companies such as Spectrum and are being modestly priced to encourage their use. However, development boards will have to be developed individually for some of the newer processors and many non-mainstream applications.

Software considerations

The design team should assess its familiarity with the most appropriate programming language. Most DSP-based designs using 16-bit processors have been implemented using assembly languages, which impact overall system performance minimally. But the newer 32-bit DSP chips can reduce the performance penalties that normally appear with the use of higher-level languages. This means that designers can increasingly consider using C with few problems.

Designers should be careful to find debuggers that will support breakpoints and other key functions of a signal-processing system. And, because data are going to be moving—sometimes rapidly—to or from remote storage once the system is on line, the designer should consider how to implement this capability.

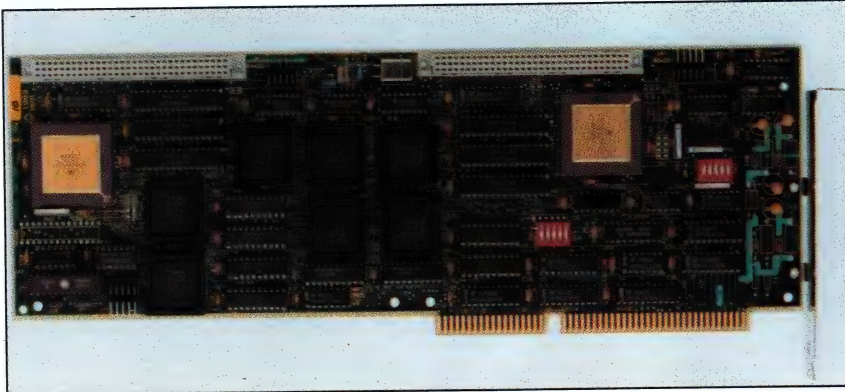
At this point in the design process, the software application libraries offered by the chip vendor or third parties should be evaluated to determine that they will be able to supply the required signal-processing routines. If not, some resources may have to be assigned to developing additional custom libraries once the design process gets underway.

On the hardware side, signal processors are still subject to a few requirements some designers will associate with microprocessors. For example, hardware emulation is often needed to assure a design's efficacy. Emulation is strongly recommended for design teams relatively new to signal processing and is almost always required in the more complex floating-point designs required for many applications.

System interface issues

System interface criteria should be evaluated at the same time or just after answering questions about the engine's features and software avail-

APPLICATION	Appropriate Data Bits	Fixed or Floating Point
GOVERNMENT/MILITARY		
Sonar (Beam forming, FFT)	32	Float
ECM (FFT, adaptive filtering)	32	Float
Airframe simulation	32	Float
Radar tracking	32	Float
(Precision FFT, matrix inversions)		
Missile guidance	32	Float
SPEECH		
Recognition	32	Float
(Feature extraction, spectrum analysis, pattern matching)		
Speaker authentication	32	Float
Synthesis	32	Float
(LPC, formant synthesis, CELP)		
Compression (LPC, cepstrum, CELP)	32	Float
— Broadband speech		
— Encryption		
HIGH QUALITY AUDIO		
Compression (QMF)	24	Fixed
Special effects	24	Fixed
Noise cancellation and reduction	24	Fixed
MEDICAL		
Compression (Acquisition, storage)	16	Fixed
Recognition	16	Fixed
(Feature extraction, pattern matching)		
IMAGE PROCESSING		
Filtering	16	Fixed
Pattern recognition	16	Fixed



A dual processor board from Spectrum Signal Processing uses a Motorola DSP56001, one of the newer DSP chips.

ability. These criteria include external memory needs, system data rates, applications for the analog-to-digital stage, and ergonomic factors like keyboard and screen interfaces.

To determine the cost effectiveness of a system, the designer should determine the amount of memory required in the application. This number should be weighed against the required access speed. Any requirement to speed up the DSP engine will take precedence and will need to be synchronized with the system's memory configuration.

If a Harvard memory architecture is chosen, the design team should determine how much the architecture impacts the complexity of the board layout. If a non-Harvard architecture is selected, designers should instead measure the effectiveness of arbitration between program memory space and data memory space.

There also are questions of ergonomic interfaces—for example, how important is screen-oriented I/O? It is wise to include a review of a processor's friendliness in keyboard-oriented I/O, which remains

the fundamental mechanism for most DSP-based applications. The obvious exceptions are speech recognition or speech enhancement systems that rely on spoken input.

Software and the system interface

As with the review of the chip's basic utility, there is also a set of questions about software within the context of the system interface. Examples: how much of it exists, and how effective or proven is it?

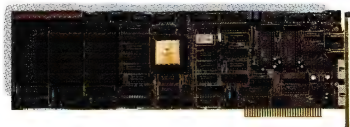
With many kinds of DSP applications, regardless of processor, some internal resources will be required to create proprietary algorithms. The design team must investigate whether a standard design tool package really will do the job.

The team must also find out about availability of component second sourcing, surface-mount capability, the strengths and overall experience of the design team with processors from the same manufacturer, and whether the design can be achieved using a two-layer board implementation. Once these questions are answered, the design team is ready to review the way the chip can or will interface in the system as a functioning unit.

EP

reprinted from **ELECTRONIC PRODUCTS** July 1990

DSP-LINK. A Unified Solution For All Of Your DSP Applications.



System Boards with Analog I/O

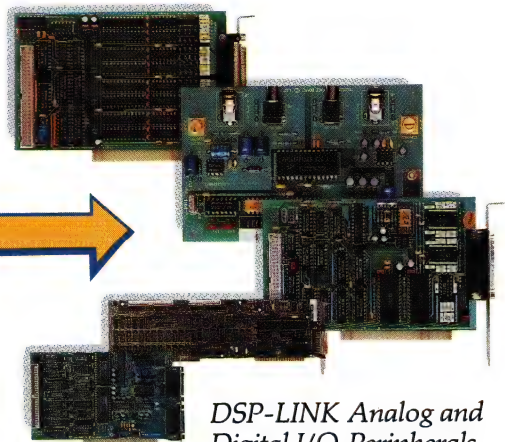


Processor Boards

Support For All Major DSP Processors:

- Texas Instruments TMS320C25/C30
- Motorola DSP56001/96002
- AT&T DSP32C
- Analog Devices ADSP-2100/2101

Development and OEM systems for Digital Signal Processing (DSP).



DSP-LINK Analog and Digital I/O Peripherals



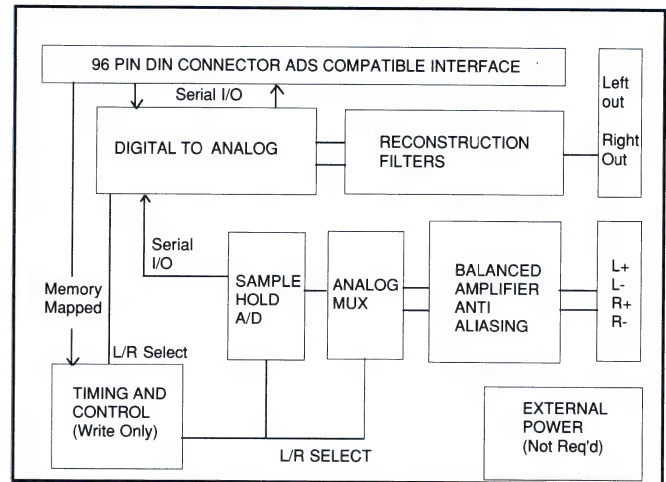
Modules for the Dual DSP56001 Processor Board

Dual Channel Analog I/O Module

Part Number: 600-00761

FEATURES

- Two channels of 16-bit analog I/O.
- 8th order elliptical anti-aliasing and reconstruction filters.
- Software programmable filter cutoff frequencies to 50 kHz.
- Software programmable sample rates up to 200 kHz on 1 channel or 100 kHz on 2 channels.
- Synchronizable to internal or external reference clock.
- Compatible plug-in peripheral for the DSP56001 Dual Processor Board or Motorola's DSP56001 Applications Development System (ADS).
- Power can be supplied from mother card or externally.
- Adjustable input and output levels from 0-100 dBm @ 600 OHMS.
- Bandlimited total distortion is less than 0.05%, signal-to-idle channel noise ratio is greater than 80 dB.
- Group delay is less than 0.4 ms.



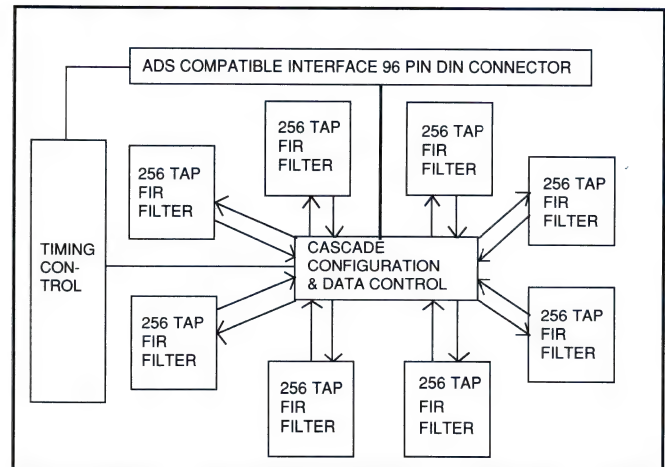
This high speed programmable analog I/O Board mates with our DSP56001 Dual Processor Board or Motorola's DSP56001 Applications Development System (ADS). The card is capable of performing 16-bit conversions at sample rates up to 200 kHz on 1 channel or 100 kHz on 2 channels. Samples are transferred serially on a DSP56001 SSI compatible bus.

Adaptive FIR Filter Module

Part Number: 600-00770

FEATURES

- General purpose Board based on Motorola's 56200 256-tap adaptive filter chip.
- Many filtering applications including acoustic echo cancelling.
- Can be software configured to any combination of adaptive and non-adaptive filters.
- Up to 2048 taps with 24 bit coefficients and 16-bit data.
- Plug-in peripheral for SPECTRUM's Dual DSP56001 Processor Board or Motorola's DSP56001 Applications Development System (ADS).
- Broadcast capability writes to more than one DSP56200 chip simultaneously.
- DSP56200's 8-bit interface is efficiently mapped onto DSP56200's 24-bit data bus.
- Low power mode is selectable when card is not in use.



The Adaptive FIR Filter Board is based upon eight Motorola DSP56200 Cascadable adaptive FIR filter chips, and mates with our DSP56001 Dual Processor Board or Motorola's DSP56001 Applications Development System (ADS).

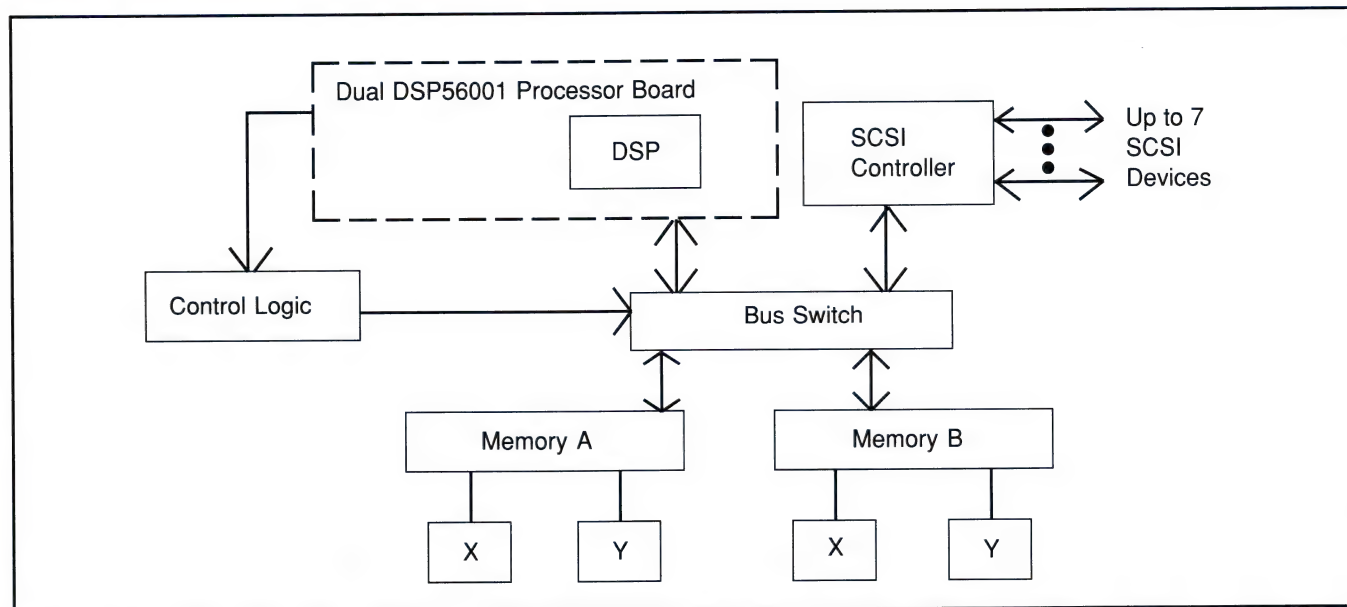
DSP~LINK Interface Module

Part Number: 600-00789

The DSP~LINK Interface Module provides the interface between the ADS 96 pin interface connector and the DSP~LINK connector. This bi-directional interface also supports a prototyping area with access to the ADS and DSP~LINK signals. The module plugs into the Dual DSP56001 Processor Board as a daughter board and allows communication from an ADS environment to/from any of the DSP~LINK peripherals or master boards.

SCSI Interface Module for the Dual DSP56001 Processor Board

Part Number: 600-01029
Advance Information



Designed to be used as a peripheral card for Spectrum's Dual DSP56001 Processor Board, the SCSI Interface Module adds the Small Computer System Interface (SCSI) capability. The SCSI Interface Module, with its high level SCSI Driver Package of software routines, provides a powerful platform for a wide range of professional audio applications and products. Applications include multimedia workstations, data acquisition systems and real-time hard disk audio recording and editing systems.

FEATURES

- Conforms to the ANSI X3.131-1986 Small Computer System Interface (SCSI) Standard
- 5 Mbyte/s SCSI Device Transfer Rate
- Supports up to 7 SCSI Devices
- Software Controlled for Maximum Flexibility and Easy Application Interfacing

DESCRIPTION

The SCSI Interface Module has been designed with dual memory banks and a dual bus architecture in order to maximize the SCSI device transfer rate while still retaining critical DSP processing power. This architecture results in true parallel processing. As the DSP writes to one memory area, the SCSI Controller is able to read from the second memory area, dramatically improving performance without cycle stealing.

Minimal DSP interaction is required to perform most SCSI operations as a high level software interface is provided for easy operation. In addition, the SCSI Interface Module can act as an initiator or as a target SCSI device for up to 7 devices.

PHYSICAL SPECIFICATIONS

Half-card daughter module for the Dual DSP56001 Processor
SPECTRUM Signal Processing Inc.

Board, which provides all the electronic circuitry for interfacing between each DSP56001 Processor and up to 7 SCSI compatible storage devices.

SOFTWARE INTERFACE

The SCSI Driver Package is a library of Motorola DSP56001 Assembler functions which provides a set of tools for using the SCSI Interface Module. These functions are intended to aid users in developing applications for the module and enable users to develop custom driver functions.

FUNCTIONAL SPECIFICATIONS

- **Reset_Cntrl:** Resets the SCSI Controller Chip on the SCSI Interface Module.
- **Reset_SCSI:** Resets the SCSI Bus.
- **Read:** Reads data from a SCSI target device to Memory.
- **Write:** Writes data from Memory to a SCSI target device.
- **Verify:** Verifies data written to a SCSI target device.
- **Write_Verify:** Writes data from Memory to a SCSI target device and then verifies the data written.
- **Seek:** Requests that the SCSI target device seek to a specified logical block address.
- **Copy:** Copy data from one SCSI device to another SCSI device or the same SCSI device.
- **Copy_Verify:** Copy from one SCSI device to another SCSI device or the same SCSI device and then verify the data written.
- **Format_Verify:** Ensures that the SCSI target device is formatted so that all data blocks can be accessed.
- **Capacity:** Requests information regarding the capacity of a SCSI target device.

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Modules for the Dual DSP56001 Processor Board

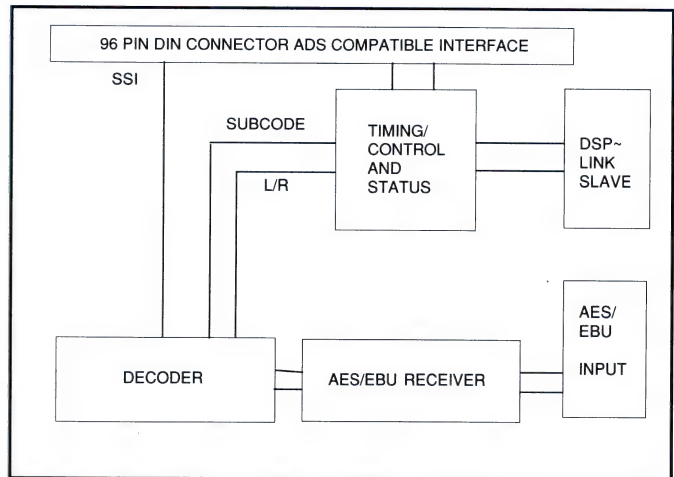
Digital Audio (AES/EBU) Receiver Module

Part Number: 600-01119

Preliminary Information

FEATURES

- Digital Audio (ANSI S4.40) compatible receiver.
- Supports stereo (L&R) reception of 32, 44.1 and 48 KHz digital audio data.
- Input to 56001 DSP processor via SSI port.
- Status monitoring for left and right data reception.
- Subcode outputs available for TX source type, copy enable/disable, emphasis on/off, sample freq.
- DSP~LINK compatible interface (slave).
- Multiple module synchronization capability.
- Compatible plug-in peripheral for the DSP56001 Dual Processor Board or Motorola's DSP56001 Applications Development System (ADS).



This digital audio receiver and DSP~LINK interface board mates with our Dual DSP56001 Processor Board or Motorola's DSP56001 Applications Development System (ADS). The card is capable of receiving stereo 16-bit digital audio data at rates up to 48,000 samples per channel each second. Samples are transmitted serially on a DSP56001 SSI compatible bus. The latching DSP~LINK (slave) allows communications to DSP~LINK master products. A DSP~LINK master interface with prototyping module (P/N 600-00789) and Pro-Audio Interface Board for AES/EBU transmission (P/N 600-00329) are also available.

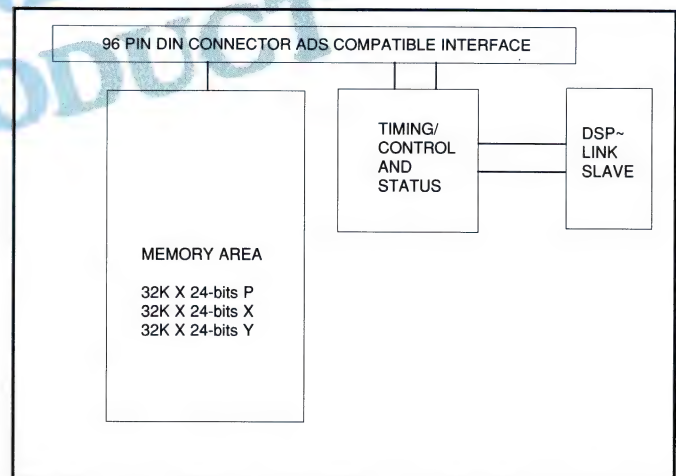
Memory Expansion Module

Part Number: 600-00957

Preliminary Information

FEATURES

- Expansion of P, X and Y memory spaces to 32K x 24-bits each.
- Zero Wait state (35ns) SRAM used.
- DSP~LINK compatible interface (slave).
- Plug-in peripheral for SPECTRUM's Dual DSP56001 Processor Board or Motorola's DSP56001 Applications Development System (ADS).



This memory expansion and DSP~LINK interface board mates with our Dual DSP56001 Processor Board or Motorola's DSP56001 Applications Development System (ADS). The expansion replaces on-board memory and uniquely decodes the P,X and Y memory spaces. The latching DSP~LINK (slave) allows communications to DSP~LINK master products. A DSP~LINK master interface with prototyping module (P/N 600-00789) is also available.

Combination Memory Expansion & Digital Audio Module

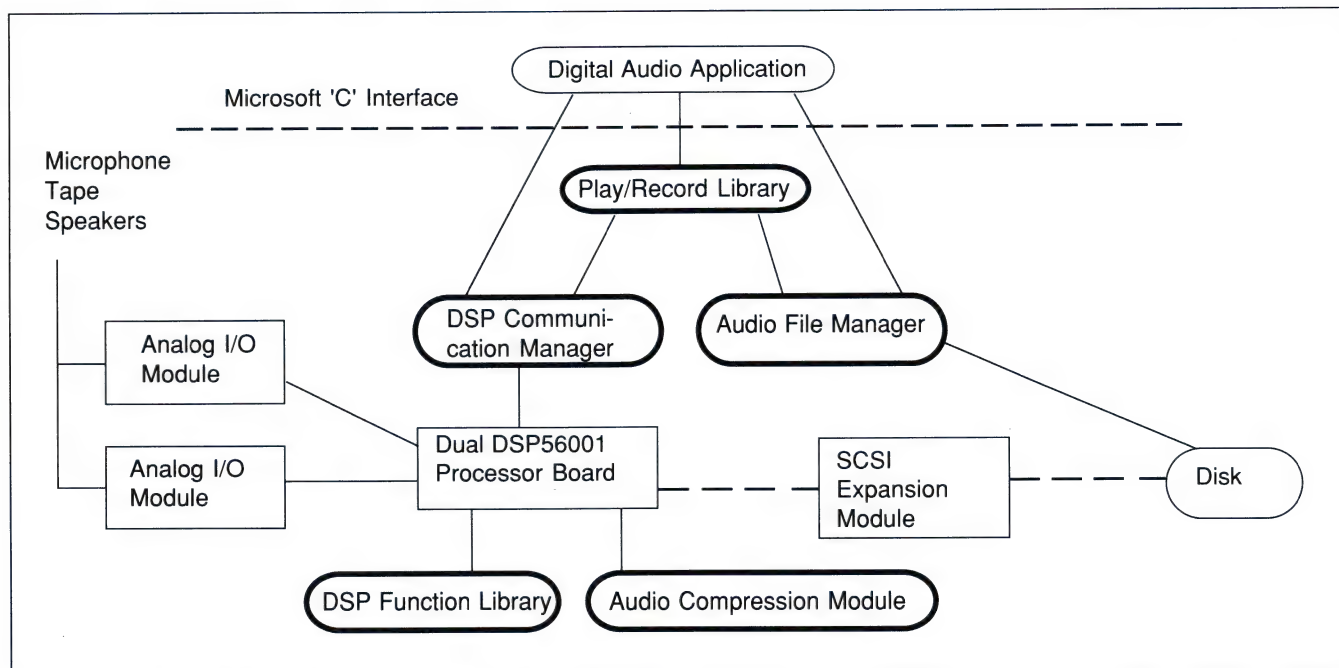
Part Number: 600-00948

Preliminary Information

This combined digital audio receiver and memory expansion module incorporates the features of the Digital Audio Receiver (P/N 600-01119) and the Memory Expansion (P/N 600-00957) modules. Included on the card is a DSP~LINK slave interface. A DSP~LINK master interface with prototyping module (P/N 600-00789) is also available.

Software for the Dual DSP56001 Processor Board

Advance Information



Digital Audio Toolkit Product Overview

Digital Audio Toolkit

Part Number: 100-00527

FEATURES

- Microsoft "C" Compatible Routines
- Sample Rates up to 48 kHz
- Stereo or Mono Recording Capability
- Fast Forward/Reverse Capability

APPLICATIONS

- Digital Audio Recording
- Audio Editing - Mixing
- Multimedia Applications

The Digital Audio Toolkit is a Microsoft 'C' compatible link library which, together with the Dual DSP56001 Processor Board and Analog I/O Module, provides a powerful set of tools for the development of disk-based audio recording and signal processing applications. The library provides all necessary functions to implement a digital audio record/playback system with audio editing features. OEM developers may use the library to develop multimedia applications, multi-track audio recording systems, audio sample editors, analysis/synthesis software, and audio signal processing applications. Functions are included for high resolution display and editing of audio waveforms, multi-track recording/playback of audio files, setting sample rates, filter cutoff frequencies, event-list management, and downloading signal processing functions to the Dual DSP56001 Digital Signal Processor Board.

Audio Compression Module

Part Number: 100-00536

FEATURES

- 15 kHz audio bandwidth at a fixed data rate of 128 kbit/s.
- Error immunity to 10^{-4}
- Low Coding Delay < 3 ms

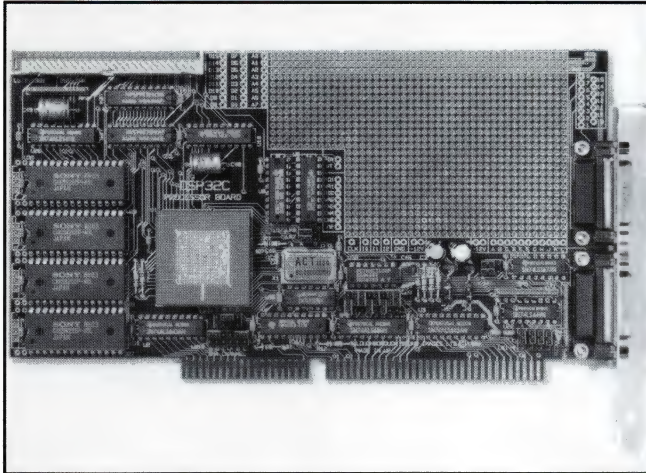
APPLICATIONS

- Broadcast Program Audio
- Digital Audio Recording
- Interactive Multimedia Terminals
- Direct Broadcast Satellite, Digital Broadcast Radio

The Audio Compression Module is a Microsoft "C" compatible link library which provides encoding of 15kHz audio signals to a 128 kbit/s data stream. Intended to be used with the Spectrum Dual DSP56001 Processor Board, the algorithms use Sub-Band ADPCM with dynamic Bit Allocation (SB-ADPCM-DBA) to achieve superior compression rates. Compared to conventional PCM coding, this advanced audio coding algorithm allows four times as much audio data to be stored on a hard disk, with no loss in subjective quality.

DSP32C Processor Board with Development Support

Part Number: 600-00662



FEATURES

- AT&T DSP32C 80ns floating point DSP.
- **DSP~LINK** System Expansion Interface.
- 40K Words (32-bit) Fast SRAM supplied.
- 136K Word on-board memory capacity (at present).
- On Board prototyping area allows user customization.
- 16 Mbps full duplex serial I/O.
- IBM PC/AT or true compatible plug-in board.
- Monitor software includes single-step, breakpoint, code disassembly and full speed operation.
- 'C' Board drivers.

The system supports the 80ns instruction cycle, comes with 8 Kwords of zero wait-state static RAM in memory area B and 32 Kwords of two wait-state static RAM in area A. Utilizing the 16-bit data path of the PC/AT bus, the board occupies just 16 locations in the PC/AT's I/O address space. Also supported

are: DMA fast transfers, bi-directional interrupts and multiple board installations.

The user prototyping area permits the addition of custom interfaces or expansions. SPECTRUM will consider producing user-custom versions of the board where sufficient volume merits it. Data can be acquired via the DSP~LINK system expansion interface. This 50-pin standardized expansion bus is featured on all SPECTRUM products including multi-channel data acquisition cards, providing users with the flexibility of tailoring a system to match its analog and digital I/O requirements.

The on-chip serial port is fully buffered and brought out to a DB15 style connector. It supports 8, 16 or 32-bit transfers at clock rates in excess of 16 Mbits per second.

DEVELOPMENT SUPPORT

The debug monitor provided is a graphic intensive, windowed format, featuring pull-down menus and mouse support. Debugging features include single step, breakpoint, disassembly, program loading, data upload/download, register inspection/modification and full speed operation.

Sample programs familiarize the user with DSP32C assembly language and give good examples of how a DSP32C-based system can be used in a PC/AT environment. In addition to these sample programs, AT&T's DSP32C Applications Library is offered, providing object code for many DSP functions including various FFT's and filter functions.

A library of 'C'-callable board drivers for the PC is provided including 'C' and assembly source code, Microsoft linkable object modules, and many examples.

• Processor

DSP32C running at a 50 MHz clock rate
(80ns instruction cycle).
32-bit floating point arithmetic.
Four 40-bit accumulators.
1536 Words (32-bit) internal RAM.

• Memory

8K x 32 of 25ns RAM in area B
32K x 32 of 45ns RAM in area A, expandable to
128K x 32.
Memory requiring 2 to 5 wait states can be supplied.

• Prototyping Area

Approximate size: 27 x 37 holes on a 0.1" grid
All appropriate signals, including DSP~LINK
are routed to the area.
+/-12V rails are LC filtered.

• Serial I/O

Synchronous, 16 Mbps.
All signals are buffered.

Clock and Sync can be internal or external.

• Host Interface

16-bit PC/AT card format.
Occupies 16 contiguous I/O ports (fully mappable).
Choice of four PC interrupts.
Full DMA implementation.

• DSP~LINK System Expansion Interface

16-bit parallel expansion bus
Up to 5 MWords/sec transfer rate.
256 memory-mapped DSP I/O ports available.
Standard 50-pin male ribbon cable connector.
DSP~LINK specifications are available for
interfacing application-specific hardware.

• Physical

Half-card format PC/AT plug-in board.
Dimensions: 8.75"L x 4.8"H x .5"D.

• Electrical

Power consumption: + 5V @ 1.2A

DSP~LINK Peripherals

Selection Guide

Description	Part No.	Analog Inputs			Analog Outputs			Programmable Filters (1)		Trigger Options (2)
		Bits	Range	Thruput (KHz)	Bits	Range	Thruput (KHz)	In	Out	
4 Channel Analog Input/ 2 Channel Analog Output	600-00185	12	±2.5V	230	12	±2.5/5.0V	300/ch	3L-R	3L-R	S,T,X
32 Channel Analog Input	600-00257	12	±2.5V	230	-	-	-	1L-R	-	S,T,X
16 Channel Analog Output	600-00428	-	-	-	12	8V, ext	225/ch	-	2L-C	S,X
16-Bit Stereo	600-00491	16	±3V	153	16	±3V	204/ch	4L-R	4L-R	S,T,X
Transient Capture	600-00464	8	±1V	20,000	-	-	-	Note 4	-	Note 5

Professional Audio Interface Boards

Description	Part No.	Clocking Options	AES/EBU Interface (3)	SONY PCM	MIDI	Cascade RAM
Pro-Audio (basic)	600-00310	32, 44.1, 48 KHz external, word sync	2 Channel / 24 bit Digital Audio I/O	-	-	-
Pro-Audio (extended)	600-00329	32, 44.1, 48 KHz external, word sync	2 Channel / 24 bit Digital Audio I/O	2 Channel 16-bits	31.25 Kbaud Opto-isolated	16 x 16

Other Interface Boards

Description	Part No.	Protocols Supported	Transfer Rate	Number of Devices
SCSI	600-01020	SCSI-1, SCSI-2	5 Mbytes/sec	7

Notes

(1) Designations indicate filter order, type, and programming component.

e.g. 3L-R: third order, low-pass, resistor programmed.

2L-C: second order, low-pass, capacitor programmed.

(2) Trigger options are: (S)oftware, Programmable (T)imer, e(X)ternal.

(3) Conforms to ANSI 4.40 (AES/EBU) format.

(4) 5th order video, Gaussian, or user configurable.

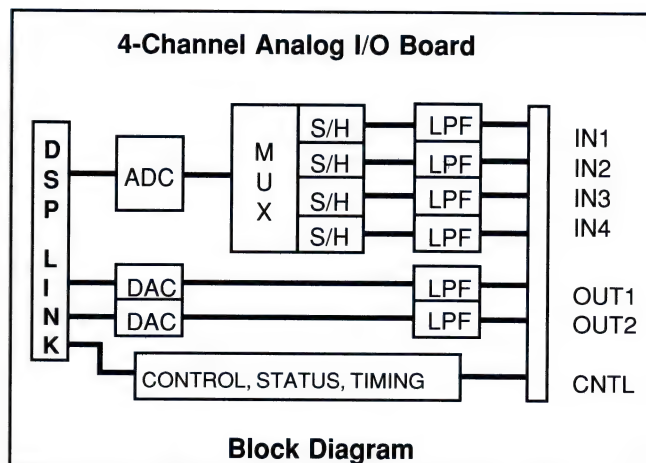
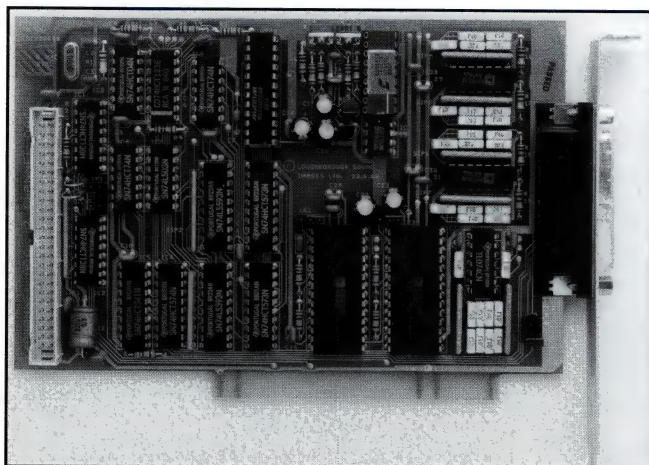
(5) External or internal with programmable sampling rate, duration, and delay.

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FEATURES

- **DSP~LINK** Data Transfer Interface.
- IBM PC/ XT/AT plug-in 'half card'.
- 4-channel synchronous sample-and-hold.
- 12-bit A/D converter.
- 3rd order filters on each input and output.
- 1-channel sampling rate up to 230 KHz .
- 4-channel sampling rates up to 58 KHz each.
- 2 output channels, fully buffered to allow simultaneous updates.
- Trigger options include on-board auto-reload counter.
- Compactly mapped to enable multiple boards on the same bus.

Four channel sample-and-hold and signal multiplexing is handled by the CS31412 chip from Crystal Semiconductor Corp. Combining the CS31412 with the Maxim 162 high-speed 12-bit A/D converter allows users a wide range of op-

tions in matching system specifications to those required. All data is two's complement, aligned to the most significant part of a 16-bit word.

An 8-bit control register determines which channel is currently in use, selects hardware or software sample triggering, controls interrupts, initiates a self calibration cycle in the CS31412, and has a user-defineable bit for controlling external circuitry via the board's interface connector on the back plate.

Sample clock rates can be generated using the auto-reload counter. This 16-bit device increments at a 8 MHz rate until overflow (FFFF). A time-out pulse is then generated and the counter automatically reloaded from a loadable register. The minimum sample rate is 122 Hz.

The two analog outputs are independently filtered and buffered to provide output drive capability.

• Analog Inputs

4 input channels (3rd order filters, programmable cutoff).
4-channel synchronous sample-and-hold (Crystal Semiconductor's CS31412).
12 bit A/D, conversion time 3 μ s (Maxim 162).
Voltage range ± 2.5 .
Single channel sampling rates up to 230 KHz.
4-channel sampling rates up to 58 KHz each.
1 user-defined digital input (read via status register bit).
10K ohm input impedance.
D-type female 25 pin connector.

• Analog Outputs

2 D/A converters, settling time 3 μ s (AD667).
Input buffers for simultaneous 2-channel output.
Selectable voltage ranges: ± 2.5 V and ± 5 V.
3rd order filters, programmable cutoff.
Output driver amplifiers for low impedance loads.
1 user-defined digital output (set via control register bit).

• A/D and D/A Trigger Options

Programmable 16-bit auto-reload counter - 8 MHz clock.
External triggering via rear connector.
Hardware or software triggering.
Timer and external triggering can interrupt DSP chip.

• DSP~LINK Data Transfer Interface

16-bit parallel expansion bus - slave.
Up to 5 Mwords/sec transfer rate.
4 DSP peripheral addresses used (mappable).
Standard 50-pin male header ribbon cable connector.

• Physical

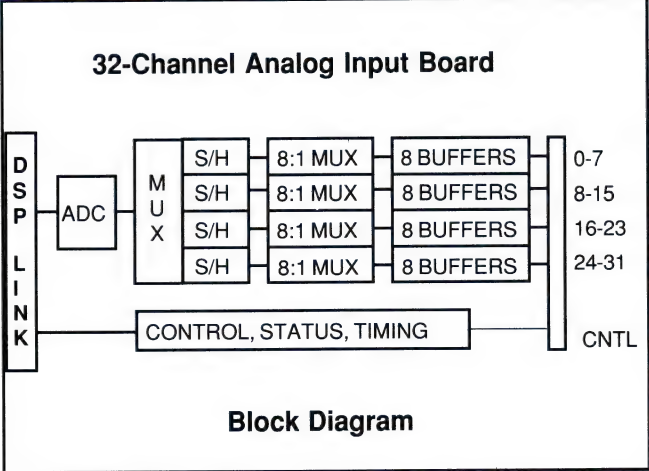
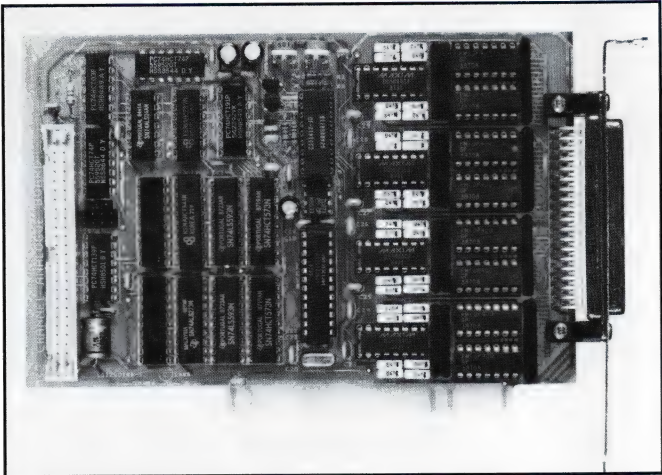
PC "Half Card" (only power is drawn from PC).
Dimensions: 7" L x 4.5" H x .5" D.
D-type female 25 pin connector for analog & I/O control.

• Electrical

Power consumption: +5V@200mA, ± 12 V@100mA each.

32-Channel Analog Input Board

Part Number: 600-00257



FEATURES

- **DSP~LINK** Data Transfer Interface.
- IBM PC/XT/AT plug-in 'half card'.
- Quad synchronous sample-and-hold.
- Four 8-channel multiplexers.
- Individual buffering and noise filtering on all channels.
- 12-bit A/D converter.
- 32-channel sampling rate exceeds 7 KHz.
- Trigger options include on-board auto-reload counter.
- Compactly mapped to enable multiple boards on the same bus.

The 32-Channel Analog Input Board provides a cost effective, flexible analog interface for systems requiring the monitoring of a substantial number of signals.

Sampling rate varies inversely with the number of channels currently in use (see throughput table). Sample clock rates

can be generated using the auto-reload counter. This 16-bit device increments at an 8 MHz rate until overflow (FFFF). A time-out pulse is then generated and the counter automatically reloaded from a loadable register. The minimum sample rate is 122 Hz.

The inputs are arranged as four banks of eight (four Maxim DG508A 8-channel multiplexers), each bank feeding an input to a 4-channel sample-and-hold/multiplexer (Crystal Semiconductor CS31412). The sample-and-holds are triggered simultaneously, providing the ADC with four 'equal phase' measurements at one time. This also allows for an arrangement of 16 differential inputs by using pairs of channels on different banks. All data is two's complement, aligned to the most significant part of a 16-bit word.

An 8-bit control register handles channel selection, interrupt enable, software device triggering, counter enable, and initiating self calibration in the CS31412.

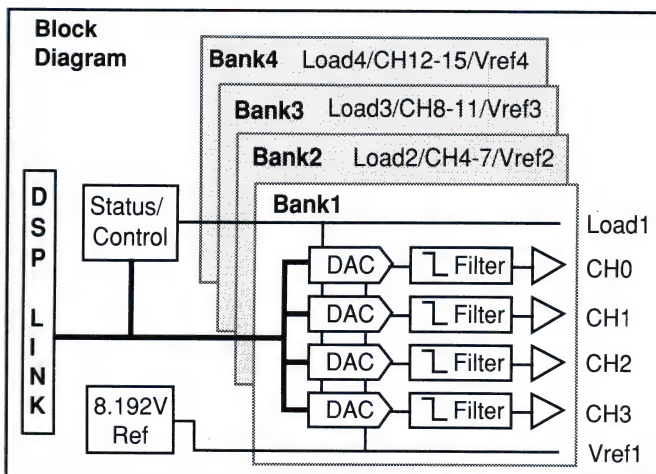
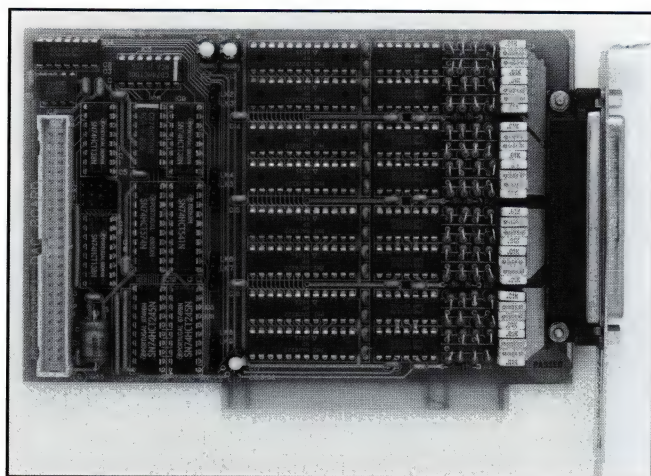
- **Analog Inputs**
 - 32 input channels.
 - 32 input buffer amplifiers.
 - 32 1st order filters (resistor programmed).
 - 4-channel synchronous sample-and-hold (Crystal Semiconductor CS31412).
 - 12-bit A/D, conversion time 3 μ s (Maxim 162).
 - Voltage range: $\pm 2.5V$.
 - Input impedance: 10K ohms.
 - D-type female 37 pin connector.
- **Trigger Options**
 - Programmable, 16-bit auto-reload counter.
 - 8 MHz crystal.
 - Software triggering enabled by a control bit.
 - Host hardware trigger.
- **DSP~LINK Data Transfer Interface**
 - 16-bit parallel expansion bus - slave.

Up to 5 Mwords/sec transfer rate.
2 DSP peripheral addresses used (may be remapped to 8 locations).
Standard 50-pin male header ribbon cable connector.

- **Physical**
 - PC "Half Card" (only power is drawn from the PC).
 - Dimensions: 7" L x 4.5"H x 0.5" D.
- **Electrical**
 - Power consumption: +5V @ 50mA., $\pm 12V$ @ 100mA

THROUGHPUT TABLE

No. channels	1	4	8	12	16	20	24	28	32
Thruput / ch. (KHz)	230	58	29	20	15	12	10	8	7



FEATURES

- **DSP~LINK** data transfer interface.
- IBM PC/XT/AT plug-in 'half card'.
- 16 independent 12-bit DACs.
- Double-buffered DAC inputs allow simultaneous analog updating.
- Simple programming.
- Two quadrant operation, four quadrant with external ref.
- On-board precision voltage reference.
- Variable voltage range via external reference.
- D/A clocking from software or from external hardware signal.

This board provides 16 independent double-buffered digital-to-analog conversion channels, each with its own capacitor-programmable, 2nd-order smoothing filter and op-amp buffered bipolar analog output. Although occupying a single 8-bit slot within the PC, only power is drawn from the PC

backplane. All control and data transfers require a separate DSP-LINK master System Board or Processor Board.

The 16 DAC channels are arranged as 4 banks of 4 channels. Each bank has a common voltage reference and a common Load Signal input, which is used to update the DAC outputs from the input registers. Users can optionally supply an external reference voltage in place of the on-board reference (for gain control, or full 4 quadrant operation). Also, the Load Signal can be generated by software, or by an external Load Pulse. Both the reference voltage and Load Signal are available as outputs if the on-board sources are used.

All DAC input registers can be written into by the controlling DSP Board by first setting an address within a Control Register, then writing the data to a Data Register. Each bank can be updated independently, or all four together, as determined by masking bits set into the Control Register. This allows different output sample rates for each bank of four channels.

• Analog Outputs

PMI DAC-2222 12-bit MDAC devices (2's complement coding).
 PMI OP471 high speed, low noise op amp on outputs.
 DAC settling time: 1 μ sec maximum.
 Op-amp settling time: 4.5 μ sec typical (filter set to highest cutoff - no caps installed).
 Outputs are protected against continuous short circuits.
 Op-amp slew rate: 8 μ sec typical.
 On-board voltage reference: + 8.192V.
 Output voltage range (load resistance: 2K ohms):
 On-board reference: + 8.188V, - 8.192V.
 External reference (approx): ± 10 V typical, ± 9 V min.

• External Voltage Reference and Load Pulse

Four quadrant operation (or external gain control) requires user-supplied reference voltages and user-controlled switching.

External reference voltage range:

Absolute maximum: ± 25 V (approx ± 10 V useful).
 External reference voltage input impedance (for each bank of 4 DAC channels): 1.5 K Ω typical.
 External Load pulse input: active low, 90 nsec.

• DSP~LINK Data Transfer Interface

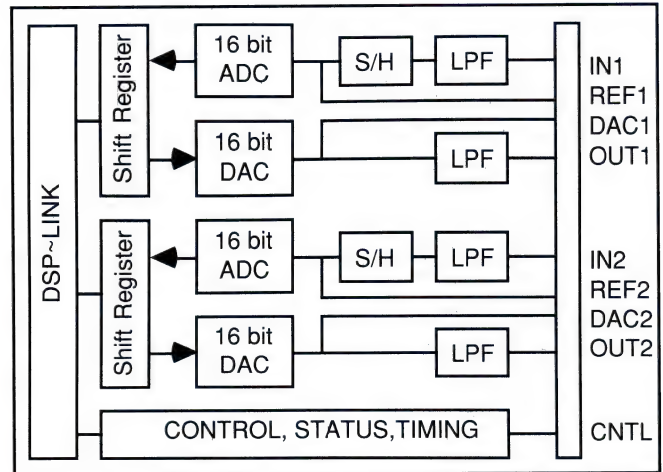
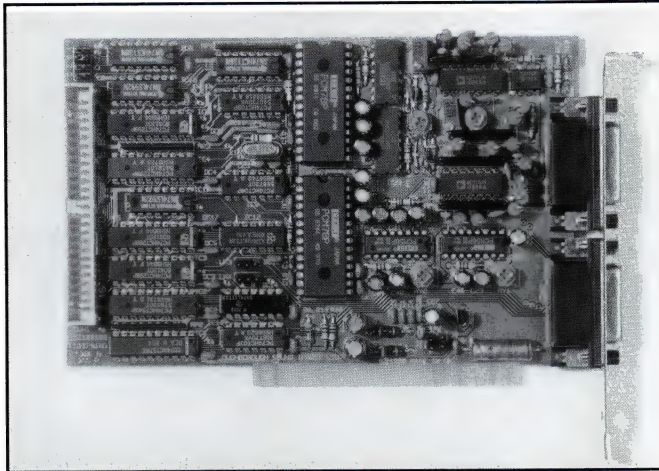
16-bit parallel expansion interface bus - slave.
 Up to 5 Mwords/sec transfer rate.
 2 DSP peripheral addresses used.
 Uses 12 most significant bits of DSP~LINK's 16-bit data bus.
 Standard 50-pin male header ribbon cable connector.

• Physical

Dimensions: 6.1" L x 3.9" H x 0.5"D.

• Electrical

Power consumption: TBD



FEATURES

- DSP~LINK Data Transfer Interface
- IBM PC/XT/AT plug-in "half card"
- Two A/D converters with Sample & Hold.
- Two D/A converters.
- 4th order filters on inputs and outputs.
- Sampling rates: 153 KHz with sample & hold. 200 KHz raw.
- Alternate sampling mode provides up to 357 KHz.
- Trigger options include on-board programmable timer.
- Compactly mapped to enable multiple boards on the same bus.

Each input channel consists of an input pre-amplifier, 4th order programmable low-pass filter, a Burr-Brown SHC5320 sample & hold (1.5 μ s) and a Burr-Brown PCM78 16-bit (5 μ s) A/D converter. Outputs use Burr-Brown PCM56 D/A convert-

ers (1.5 μ s), 4th order programmable low-pass filters and buffer amplifiers.

The conversion devices are designed for serial communication with a CPU. Since DSP~LINK is a 16-bit parallel format, each of the board's analog I/O channels includes a 16-bit shift register which receives data from the A/D as well as transmits data to the D/A.

An 8-bit control register handles channel enabling, interrupt enabling, timer control and has two general purpose bits whose signals appear at the rear connector. These can be used for control of external devices.

Sample clock rates can be generated using the on-board programmable timer. This 16-bit device increments at a 10 MHz rate until overflow (FFFF). A time-out pulse is then generated and the counter is automatically reloaded from programmable register. The minimum sample rate is 153 Hz.

• Analog Inputs

Two 4th order filters (resistor programmable cutoff).
Two sample & holds (Burr-Brown SHC5320, 1.5 μ s).
Two 16 bit ADCs (Burr-Brown PCM78, 5 μ s).
2-channel sampling rates up to 153 KHz.
Alternating channel sampling rates up to 357 KHz.
Two user-defined digital inputs (read via status register).
10Kohms input impedance.
D-type 15 pin connector.
Voltage range: $\pm 3V$.

• Analog Outputs

Two 16 bit DACs (Burr-Brown PCM56, 1.5 μ s)
Two 4th order filters (resistor programmable cutoff).
Voltage range: $\pm 3V$.
Two user-defined digital outputs (set via control register).
Output buffer amplifiers.

• A/D and D/A Trigger Options

Programmable 16-bit auto-reload counter - 10MHz clock.

External triggering via rear connector.

Software triggering via control port.

Timer and external triggering can interrupt DSP board.

• DSP~LINK Data Transfer Interface

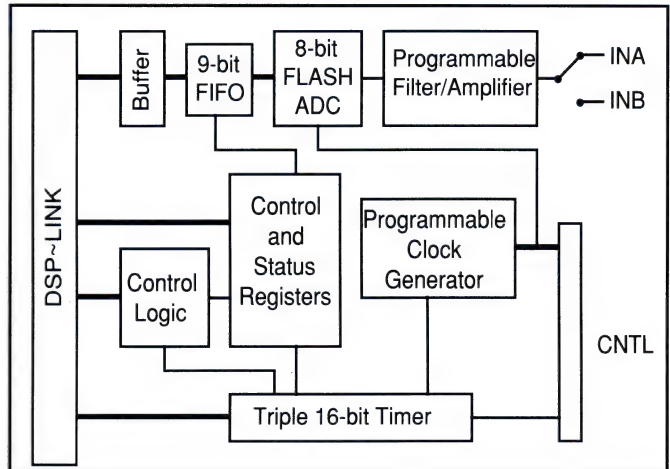
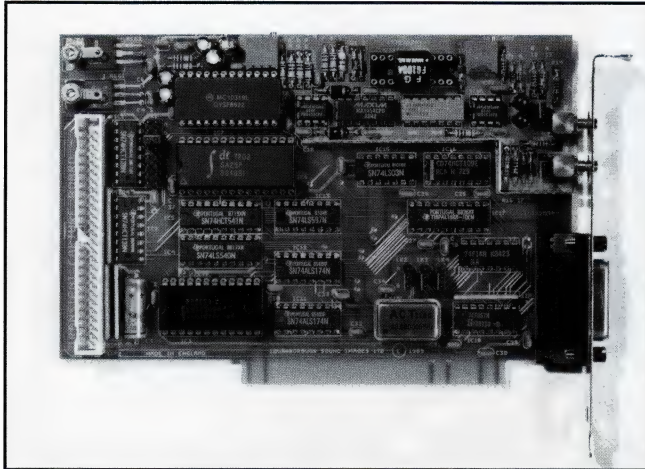
16-bit parallel bus connects this board to DSPmaster.
Up to 5 Mwords/sec transfer rate.
Board occupies 4 DSP I/O addresses (mappable).
Standard 50-pin male header ribbon cable connector.

• Physical

PC "Half Card" (only power is drawn from PC).
Dimensions: 7"L x 4.5"H x .5"D.
D-type female 15 pin connector for analog signals.
D-type male 15 pin connector for control signals.

• Electrical

Power consumption: +5V @ 200mA, $\pm 12V$ @ 100 mA each. Optional: $\pm 12V$ may be supplied externally via control connector.



FEATURES

- DSP~LINK Data Transfer Interface
- IBM PC/XT/AT plug-in "half card"
- Sampling in excess of 20 Msamples per second
- Two software multiplexed inputs can be configured to present 50 ohm or 1 Kohm resistive loading
- Software programmable gain control
- 20-pin DIP socket provides for a range of 5th order video, gaussian (supplied standard) or user configurable filters
- 8-bit flash ADC with overflow saturation
- 1, 2, 4, or 8K words deep 9 bit wide FIFO

The Transient Capture Board provides a high-speed data acquisition facility for limited periods at sampling rates in excess of 20 Msamples per second. Samples are fully buffered by means of a FIFO so that acquisition and sample READ opera-

tions are fully asynchronous. Various modes of operation are supported including internal or external trigger generation, sampling clock source and overall periodicity control.

The board is designed for applications such as line scan image capture, digital storage oscilloscope with processing, NMR scanning, and ultrasonic non-destructive testing for received echo analysis. To permit high speed processing of these signals, the Transient Capture Board will connect to SPECTRUM's DSP System and Processor Boards via the DSP~LINK data transfer interface.

A plug-in crystal oscillator provides a 40 MHz reference frequency which feeds a programmable divider to give sampling rates of 20, 13.33, 10 and 8 Msample/sec. A facility is provided for shifting the sampling phase by 1/2 clock cycle such that apparent sampling rates in excess of 40 Msample/sec can be achieved on repetitive waveforms. An external clock input allows other rates to be provided.

• Analog Inputs

Two software multiplexed inputs.
50 ohm to 1 Kohm resistive loading.
One 20-pin DIP socket for a range of plug-in filters.
One 8-bit flash ADC with overflow protection (Motorola MC10319L).
Sampling in excess of 20 Msamples per second.
Voltage range: $\pm 1V$.

• A/D Trigger Options

Internal trigger generation via 3 on-board timers:
Trigger Period Timer - time between trigger events;
Trigger Delay Timer - time between trigger event and commencement of sampling;
Sampling Period Timer - time over which samples are stored in the FIFO.
External triggering via control input.

• Control Connector

Permits full control of sampling rates, trigger events sampling periods.

• FIFO

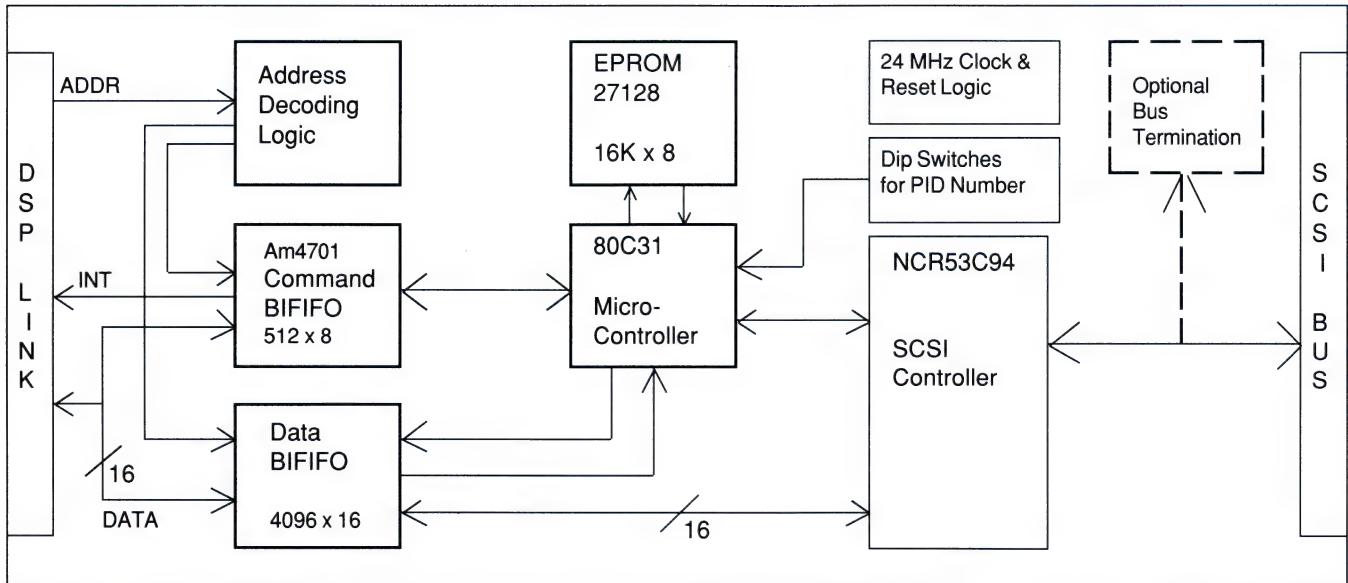
1, 2, 4, or 8K words deep FIFO.
9-Bit wide FIFO, 9th bit can be used:
to indicate overflow or saturation;
to indicate start or end of sequences;
to identify captured samples by a serial code.
Samples from the FIFO are sign-extended to 16-bits for communication over DSP~LINK.

• DSP~LINK Data Transfer Interface

16-bit parallel bus connects this board to DSP master.
Up to 5 Mwords/sec transfer rate.
Board occupies 4 DSP I/O addresses (mappable).
Standard 50-pin male header ribbon cable connector.

• Physical

PC "Half Card" (only power is drawn from the PC).
Dimensions: 7"L x 4.5"H x .5"D.
Two mini-BNC connectors for analog input.
D-type male 15-pin connector for control signals.



FEATURES

- DSP~LINK Data Transfer Interface.
- IBM PC/XT/AT plug-in 'half-card'.
- Uses NCR53C94 Advanced SCSI Controller along with an 8031 Microcontroller.
- Compatible with both SCSI-1 and SCSI-2 protocols.
- Up to 5 Mbytes/sec SCSI data transfer rate.
- Supports up to 7 SCSI bus devices including hard disks, optical scanners, and CD-ROMs.
- Facilitates multi-processor communications.
- Compactly mapped to enable multiple peripheral boards on the same DSP~LINK bus.

The SCSI Board provides the capability to communicate with SCSI peripheral devices such as hard disks, optical scanners, and CD-ROMs. The board implements both the SCSI-1 and SCSI-2 protocols using standard 8-bit parallel data transfers and single ended bus drivers. Although the FAST SCSI and WIDE SCSI options are not supported, data rates up to 5 Mbytes/sec are possible. Up to 7 devices can be connected to the SCSI bus. DIP switches are used to select the PID (Physical Identity) number of each device. Since the SCSI bus supports multiple master and slave devices, it is well suited for

multi-processor communications. All Spectrum DSP boards that incorporate the DSP~LINK expansion connector are compatible with the SCSI Board.

The board uses three 50 pin headers. One is for the DSP~LINK interface and the other two are for the SCSI bus. The SCSI bus connector at the outer edge of the card allows connection to peripherals external to the PC whereas the other SCSI connector allows connection to peripherals internal to the PC. An optional bus termination resistor pack can be inserted into a socket if the interface is to be used at only one end of the SCSI bus.

The main components of the SCSI Board are a NCR53C94 Advanced SCSI Controller interface chip, a 8031 microcontroller, and two bi-directional FIFO memory chips. The 8031 microcontroller, executing from EPROM, performs all the low level housekeeping required by the NCR53C94. A 512 stage, 8-bit, bi-directional FIFO is used for transferring command and status information between DSP~LINK and the 8031. A separate 4096 stage, 16-bit, bi-directional FIFO is used for data transfers between DSP~LINK and the NCR53C94. These two BIFIFOs occupy four contiguous locations in the DSP~LINK memory address space.

• SCSI Hardware

SCSI-1 and SCSI-2 compatible.
Up to 5 Mbyte/sec synch/asynch transfer rate.
NCR53C94 Advanced SCSI Controller.
8031 Microcontroller.
512 stage 8-bit BIFIFO for communication between DSP~LINK and 8031 Microcontroller.
4096 stage 16-bit BIFIFO for data transfers between DSP~LINK and NCR53C94 SCSI Controller.
Two standard 50-pin male header ribbon cable connector for SCSI devices.

• DSP~LINK Transfer Interface

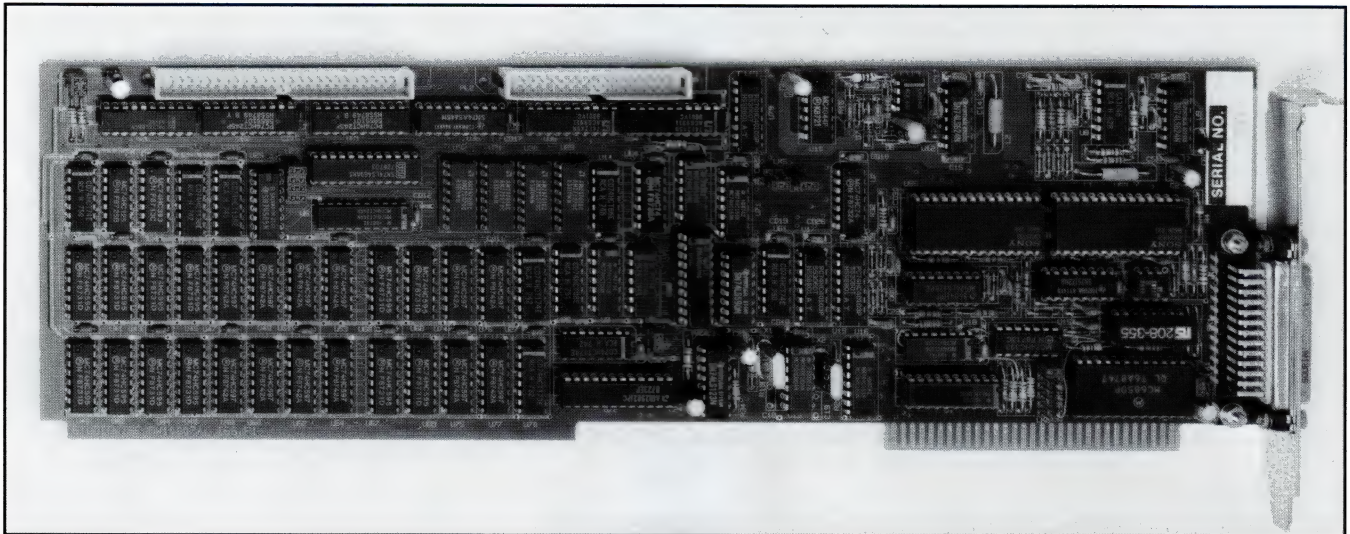
16-bit parallel expansion bus - slave.
Up to 5 Mwords/sec transfer rate.
4 DSP peripheral addresses used (re-mappable).
Standard 50-pin male header ribbon cable connector.

• Physical

PC "Half Card" (only power is drawn from the PC).
Dimensions: 7"L x 4.5"H x 1/2"D.

• Electrical

Power consumption: TBD



FEATURES

- **DSP~LINK** Data Transfer Interface.
- IBM PC/XT/AT plug-in board.
- Industry standard ANSI 4.40 (AES/EBU) serial interface for digital audio.
- Supports previous industry standard SONY PCM format.
- 32 KHz sample clock for digital broadcast systems.
- 44.1 KHz sample clock for CD and DAT systems.
- 48 KHz sample clock for professional digital studios.
- Various word-sync options provide adaptability to virtually any system configuration.
- Industry standard MIDI interface.
- Cascadable (up to 16) for multi-channel, multi-processor architectures.
- Compactly mapped to enable multiple boards on the same DSP~LINK bus.
- Full user control of status bits, facilitating 'subcode' support.

The Pro-Audio Interface Board provides a complete digital audio communications interface for any of SPECTRUM's **DSP~LINK** Master Boards.

Supporting both AES/EBU and SONY PCM serial data formats as well as MIDI, the Pro-Audio Interface Board is the bridge between existing professional digital audio equipment and SPECTRUM's wide range of Digital Signal Processing products.

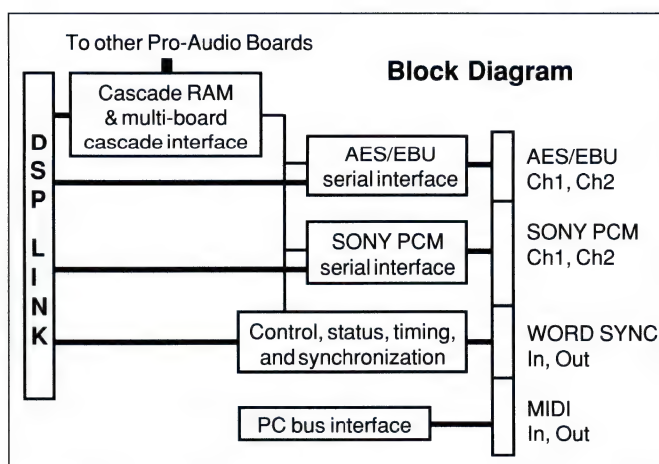
This combination puts the necessary hardware and development tools in the hands of digital audio system designers at an affordable price.

Synchronization of data (word-sync) can be driven by an on-board clock generator, producing the standard 32, 44.1, and 48 KHz rates. Word-sync can also be recovered from incoming ANSI audio data, or driven by an external TTL reference. Any word-sync option can be shared among cascaded Pro-audio boards.

The Cascade RAM and Cascade Bus comprise a medium for connecting multiple Pro-Audio Boards together with common synchronization. The RAM areas are arranged similar to a 'global' memory array, allowing shared data among multiple boards and simplified multi-processor communications.

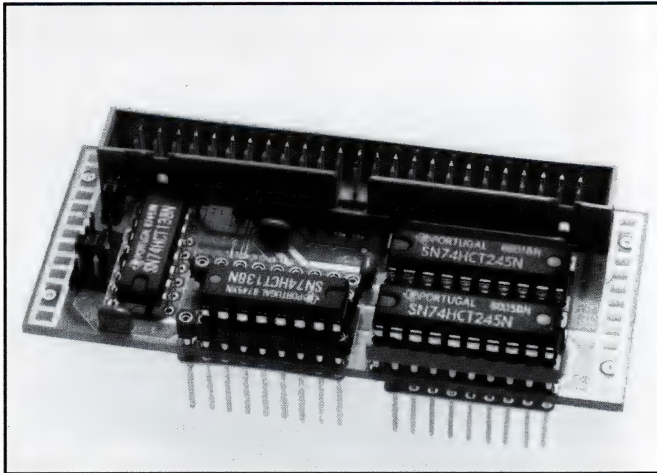
The MIDI interface is the only function of the board which is accessed directly by the host PC rather than the DSP master board. Implementing the 31.25 Kbaud serial communications standard is a Motorola MC6850 UART device, mapped into the PC's I/O space. Facility is provided for PC interrupts, the particular interrupt to be used being link selectable (IRQ2-7).

The Pro-Audio Interface Board comes in two versions. The extended version includes all the features described above. The basic version does not include the SONY PCM, MIDI, or cascade RAM features.



DSP~LINK Prototyping Module

Part Number: 600-00338



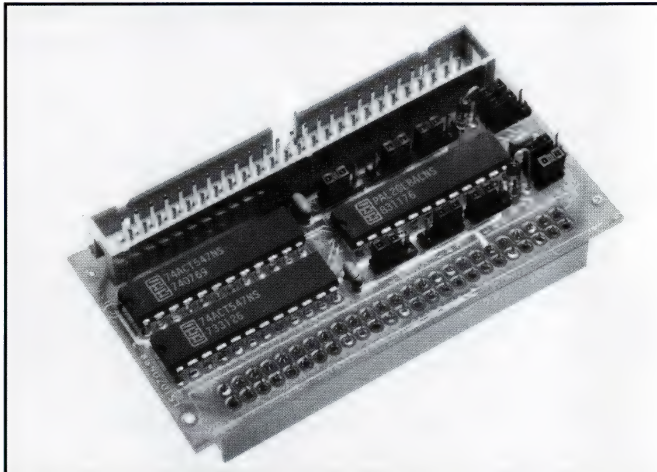
The Prototyping Module is a small circuit board designed to be placed on a user-supplied wirewrap prototyping board. This module provides the capability to quickly design a custom interface via DSP~LINK for any of Spectrum's System or Processor Boards.

The module provides bi-directional data buffering, address and control signal decoding for up to four of the 16 possible I/O ports on DSP~LINK. Jumpers can be used to select one of four possible I/O port base addresses. Power can be taken from DSP~LINK or from the user prototype.

The module is connected to the System or Processor (master) Board via a 50-pin ribbon cable. Connection to the user prototype is via wirewrap pins on the back of the module.

Dual-Processor Communications Module

Part Number: 600-00347

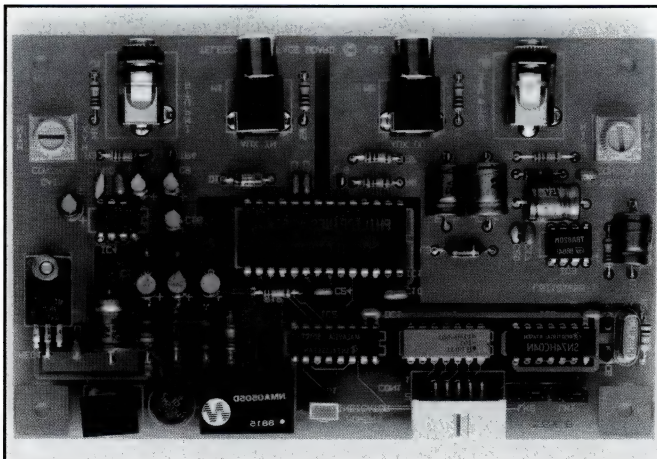


The Dual-Processor Communications Module is a small circuit board that allows communication between two DSP~LINK System or Processor (master) Boards. The module plugs into the DSP~LINK connector of one master and connects to the other via ribbon cable. Since the module uses two DSP~LINK I/O ports, more than one may be connected to a master board, allowing multiple processors to communicate. Data transfer rates of up to 3 Megawords per second are possible.

The module implements a simple bi-directional latching register that can be used as a "mailbox" between two DSP's. Handshaking can be done using interrupts, polling, unique 16-bit data patterns, or a combination of these techniques. With minor customizations, the module can be used as a general-purpose parallel input or output port (to drive LEDs, sense switches, communicate with existing equipment, etc.).

Linear Codec Module

Part Number: 600-00563



The Linear CODEC Module is a low cost, stand-alone analog subsystem based upon Texas Instruments' TLC32040 analog interface chip. It interfaces to most SPECTRUM DSP System and Processor boards via their synchronous serial ports. Intended for voiceband applications, the module includes a variable gain microphone pre-amplifier, as well as an output power amplifier for driving an external speaker. The TLC32040 incorporates a switched capacitor input filter, a 14-bit A/D converter, 14-bit D/A converter, switched capacitor reconstruction filter, as well as its serial interface. Sampling rates and filter bandwidths are programmable. The device input has a linearity of 10 bits. Power is supplied using an external plug-mounted transformer. The Linear CODEC Module regulates this incoming power on-board. Example programs are provided in assembly language to demonstrate simple implementations of this analog interface.

VME & Futurebus+ Boards

Selection Guide

Product	DSP56001 VME Board	Dual TMS320C30 VME Board	Versatile Array Signal Processor (VASP)		
			I/O Processor Board	General Signal Processor Board	Two Port Memory Board
Part Number	600-00446	600-01002	600-00966	600-00975	600-00984
Form Factor	6U VME	6U VME	6U VME/ Futurebus+ ⁽¹⁾	6U VME/ Futurebus+ ⁽¹⁾	6U VME/ Futurebus+ ⁽¹⁾
Processors	1 DSP56001	2 TMS320C30	1 DSP96002	4 DSP96002	N/A
Instruction Cycle	100ns	60ns	60ns	60ns	
Precision	24-bit integer	32-bit floating pt.	32-bit floating pt.	32-bit floating pt.	
Accumulators	2 x 56-bit	8 x 40-bit	1 x 32-bit	1 x 32-bit	
Internal Memory	1024 Words	2048 Words 64 Word CACHE	1024 Words (Pgm) 1024 Words (Data)	1024 Words (Pgm) 1024 Words (Data)	Configurable up to 32 Mbytes Dual Ported Memory
On-Board Memory					
Standard	24K x 24	64K x 32 (Local) 256K x 32 (Global)	32K x 32	64K x 32 per Processor	
Maximum	128K x 24	256K x 32 (Local) 4M x 32 (Global)	32K x 32		
Serial I/O	1 Synch (5 Mbps) 1 Asynch (RS-232)	2 Synch (8.33 Mbps)	None	None	None
Parallel I/O Interface	None	DSP~LINK	32-bit (10 MHz)	None	None
Expansion Bus	None	32-bit, 16.67 MHz	64-bit (Data), 32-bit (Addr.), 50 Mbytes/sec		
Analog I/O					
Channels	2 channels I/O	2 channels I/O	None ⁽²⁾	None ⁽²⁾	N/A
Resolution	16-bit	18-bit			
Max. Sampling Rate	153 KHz/ch	200 KHz/ch			
Application Software					
Real-Time O.S.	None	SPOX™	None		
C Compiler/Assem.	Motorola	TI	Motorola/Intermetrics		

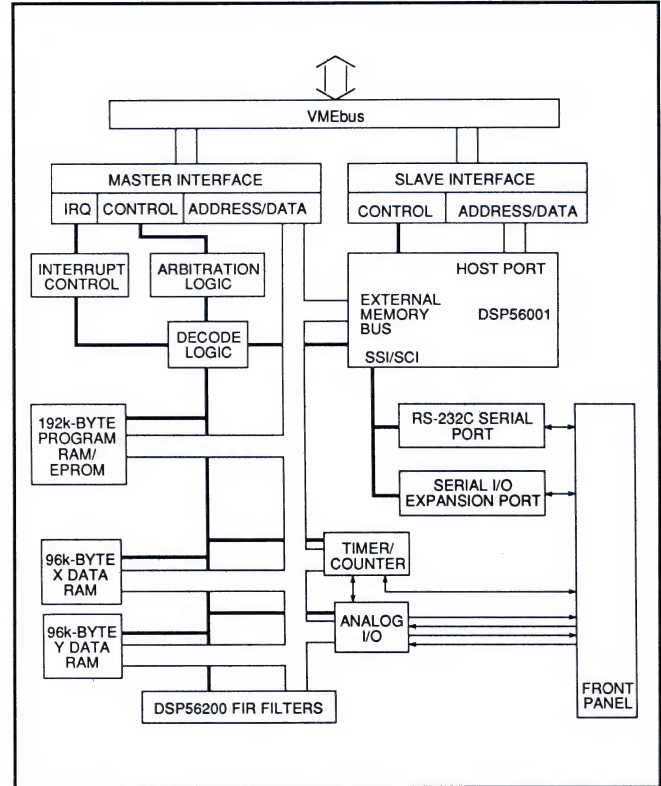
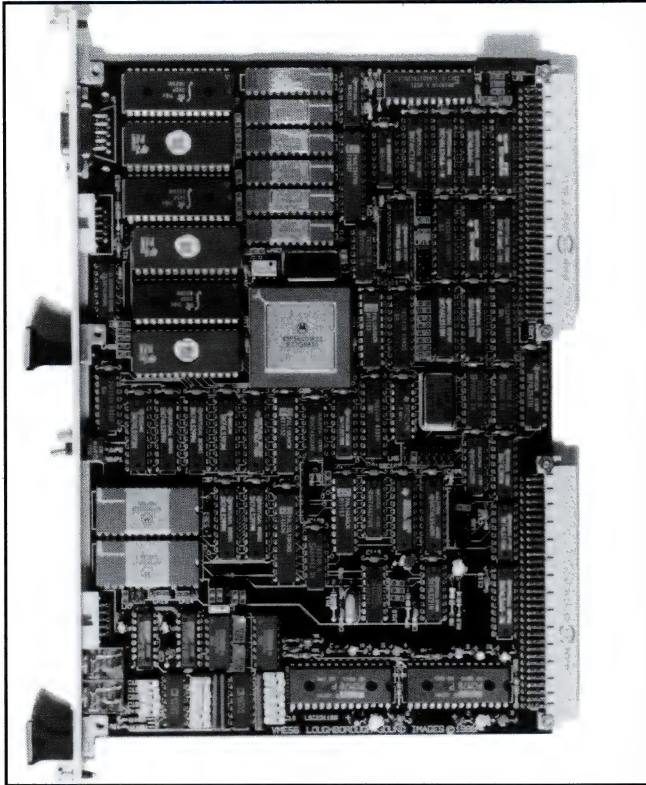
Footnotes:

(1) These boards use a Futurebus+ physical connector and a SPECTRUM VME/Futurebus+ proprietary backplane (Part Number 600-01137) to connect VASP processing stages and to interface to VME compatible boards.

(2) Standard VME analog I/O boards may be accessed using the VME/Futurebus+ backplane (part number 600-01137).

DSP56001 VME Board with Development Support

Part Number 600-00446



The DSP56001 VME Board is a high performance digital signal processing (DSP) system designed for compatibility with the VME C.1 bus specification. The board's processing power is provided by a Motorola DSP56001 single chip DSP, as well as two Motorola DSP56200 adaptive FIR filter processors.

FEATURES

- Motorola DSP56001 24/56 bit, 100ns processor.
- Two Motorola DSP56200 digital FIR filter processors.
- 128 Kword on-board memory capacity.
- Two high-speed 16-bit ADCs and DACs.
- High speed synchronous serial communications interface.
- RS-232 asynchronous serial communications interface.
- Software development environment for Sun Workstation.
- PC-based development environment via RS-232.
- Unix drivers provided

All three processors are running at 10 MIPS (million instructions per second), and are able to execute the DSP-critical Multiply/Accumulate instruction in a single 100ns cycle. The board is supplied with 8 Kwords of zero wait state (35ns) RAM in each memory area X, Y and P. Program memory area can be upgraded to 64 Kwords, while X and Y areas can each be upgraded to 32 Kwords. As shipped, program area is also occupied by 8 Kwords of EPROM which carries the portion of the PC-based debug monitor which runs on the DSP56001.

SPECTRUM Signal Processing Inc.

Eastern US: (508) 366-7355 or 800-323-1842

Western US: 800-663-8986

Canada: (604) 438-7266

The DSP56001 VME Board can acquire and create analog signals via two high-speed A/D and D/A channels, which are mapped into the processor's I/O space and are fully independent of the VME bus interface. This reduces burden on the VME bus of transferring unprocessed analog data. If necessary, however, VME bus-based data acquisition cards can also be used in conjunction with the board.

The DSP56001's two full duplex serial ports are made available at the endplate, the SSI being buffered and configurable for up to 5 Mbps synchronous communication. The SCI asynchronous port is implemented as RS-232.

DEVELOPMENT SUPPORT

DSP software development can be carried out either in a Sun 3 environment, or on an EGA-equipped PC compatible (PC communicates with the board via RS-232). In either case, the debug monitor software is windowed, featuring "examine & modify" windows for disassembled code, as well as data memory and registers. Downloaded programs can be run in real time, with and without breakpoints or single-stepped.

Example programs familiarize the user with DSP56001 assembly language as well as communication with off-chip peripherals. These examples include a variable framesize FFT, low and high-pass FIR filters running on the DSP56200's, and analog interface demonstrations.

A library of callable UNIX device drivers is provided to allow communications and control of the board over the VME bus.

- **DSP56001 Processor**

20 MHz clock rate (10 MIPS).
24-bit processing with 24 x 24 hardware multiplier and two 56-bit accumulators.
512 words (24-bit) internal data RAM.
512 words (24-bit) internal program RAM.
Four (4) data busses.
Internal ROM contains ulaw/A-law to linear and sine tables.

- **DSP56200 Processors**

10 MHz clock rate (10 MIPS).
24 x 16-bit multiplication with 40-bit accumulation.
256 x 24-bit coefficient RAM.
256 x 16-bit data RAM.
Applications: Two 32 tap, 220 KHz FIR filters
One 64 tap, 220 KHz FIR filter

- **Memory**

System comes with 24K x 24 of 35ns RAM
(8K x 24 in each of PGM, X, and Y).
Supports up to 128K x 24 of on-board memory
(64K x 24 in PGM, 32K in each of X and Y).
Software selectable wait-states for slower RAM or EPROM.

- **Analog Inputs**

Two 16-bit ADCs with sample-and-hold, 153KHz through-put [Burr-Brown PCM78 (5us) and SHC-5320 (1.5us)].
Third order filtering (resistor programmable).
Double-buffered data latching.
Voltage range: +/- 3V.
Type of connectors: 3.5mm stereo jacks.

- **Analog outputs**

Two 16-bit DACs [Burr-Brown PCM56 (1.5us)].
Third order filtering (resistor programmable).
Double-buffered data latching.
Voltage range: +/- 3V.
Type of connector: 3.5mm stereo jacks.

- **Analog I/O clocking options**

Software-initiated conversions.
16-bit timer initiated (minimum sample rate 153 Hz).
External timer clocking.
Timer can interrupt 56001.

- **Serial I/O**

Two I/O channels with internal/external clocks.
Synchronous: (SSI) 5.0MHz with 10-pin connector on end plate.
Asynchronous: RS-232.

- **VME Bus Master**

VMEbus specification 'C.1' compatible.
VMEbus system controller - SYSRESET, SYSCLOCK.
VMEbus interrupter.
D08(0)/D16/D32 (unaligned), A24 bus interface 8 Mbytes/ second maximum transfer rate (2.66 Mwords/sec)
Single level vectored interrupt handler (jumper selectable)
Single level bus arbiter (level 3).
Hardware wait state generation (DTACK - true asynchronous).

- **VME Bus Slave (56001 host port)**

D08(0), A16 bus interface.
5 Mbytes/second maximum transfer rate.

- **Physical**

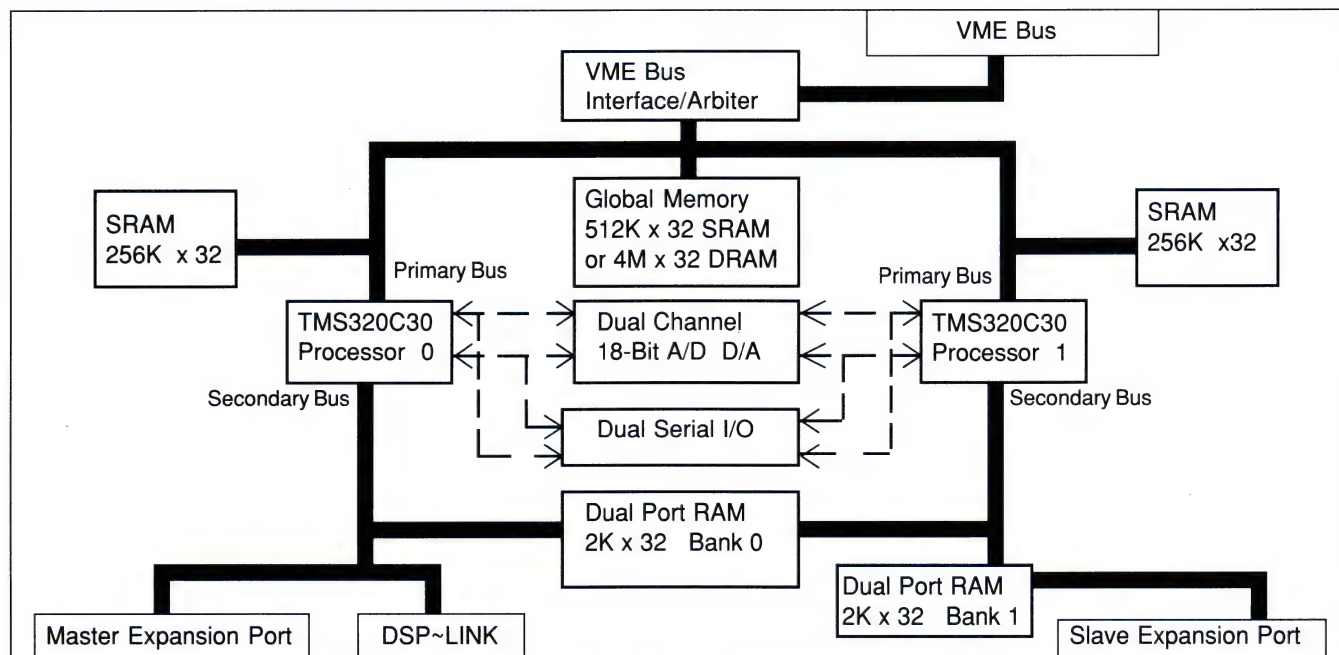
6U VME bus card.

- **Electrical**

Power consumption:
+ 5V @ 2A
-5V @ 100mA
+12V @ 100mA
-12V @ 100mA

Dual TMS320C30 VME Board with Development Support

Part Number: 600-01002
Preliminary Information



FEATURES

- 66 MFLOPs computing power on a single 6U VME module.
- Two processing nodes, each incorporating a TMS320C30 processor and up to 256K x 32 fast SRAM.
- Up to 512K x 32 SRAM or 4M x 32 DRAM global memory array.
- Two channels of 18-bit A/D and D/A (optional).
- Two high speed synchronous serial ports.
- Two banks of 2K x 32 dual port RAM for zero overhead data transfers between processing nodes.
- Master and slave 32-bit bidirectional parallel ports for connecting multiple boards together.
- DSP~LINK parallel expansion for connecting to peripheral I/O boards.
- VMEbus rev C1 slave interface.

The Dual TMS320C30 VME Board is a 6U Eurocard which plugs directly into a single slot on a VME backplane. The board is designed to provide a powerful general purpose digital signal processing system for the VMEbus.

The architecture of the board centers around two Texas Instruments TMS320C30 processors, each capable of computing 33 million floating point operations per second. To maximize program execution speeds, each processing 'node' has its own local SRAM store of 64K x 32 operating with zero wait-states. The use of SIMMs enables this memory area to be expanded to 256K x 32 without any loss in performance. In addition to local SRAM, both processors have shared access to an area of global memory which is also dual-ported with the VMEbus. This area can be fitted with up to 512K x 32 of zero wait-state SRAM or, using a daughter card, up to 4M x 32 of

three wait-state DRAM. Data can be transferred between global memory and each C30's local SRAM using the C30's DMA controller. In this way, regular node processing is not affected by global memory data transfers.

The board is equipped with three parallel, bidirectional expansion interfaces: a 32-bit master, a 32-bit slave, and DSP~LINK. Each bidirectional interface supports high speed communications via a 50-way ribbon cable connector. The 32-bit master and slave expansion interfaces provide a communications interface for multiple Dual TMS320C30 VME Boards configurations. The 16-bit DSP~LINK interface allows users to interface to their own peripheral I/O boards.

The board's multi-processing architecture has been optimized using dual ported memory mapped into the secondary memory space of each processing node. A block of 2K x 32 of DPRAM occupies the same address space of both processors, enabling one processor to transfer data to the other by simply reading or writing memory as part of normal program execution. A further 2K x 32 block of DPRAM, shared between processor '1' and the a DPRAM access port, facilitates ring and star multiprocessing topologies.

The board has an A32 D32 VMEbus slave interface and is compatible with revision C1 of the VMEbus specifications. D16, D08(O), D08(E0), and BLT capabilities are also provided. The board memory and registers are mapped into a user selectable 2M word region on the VMEbus. Either C30 processor may interrupt the VMEbus. The single level interrupt generator, when selected to participate in an interrupt cycle, responds with an 8-bit STATUS/ID vector. The VMEbus may interrupt either of the C30 processors via the control registers.

An optional feature for stand-alone applications is a two channel analog signal interface using 200 KHz 18 bit A/D and D/A converters. Analog signals with bandwidths up to 100 KHz can be acquired, processed, and output from the board in real-time. Both 4th order anti-aliasing and reconstruction filters are used.

The board contains two serial channels which may be allocated, along with the channels of A/D and D/A conversion, to either of the serial ports of each processor. Once allocated, the buffered serial expansion links directly to the selected processor serial port.

DEVELOPMENT SUPPORT

Programs can be developed using either C or TMS320C30

assembler. Both the SUN3 and SUN4 are supported as development platforms with assembler, compiler, and high level debug tools available for both.

The SPOX™ DSP operating system which includes an applications programming interface and a real-time multitasking kernel is also available to enhance C programs for real time DSP without detailed knowledge of the underlying hardware. Board drivers are available for integrating the Dual TMS320C30 VME Board into a real-time operating system under VxWORKS, OS9, PSOS, or VRTX.

UNIX drivers are also provided for SUN OS v4.1. Source code for the drivers is provided without charge to enable customers to modify them for use in their own systems.

• Processors

Two TMS320C30s operating at 33 MHz.

• Local Memory (each node)

Primary Bus: 64K x 32 0ws SRAM, expandable to 256K x 32.

Secondary Bus: 2K x 32 DPRAM accessible to both processors and 2K x 32 DPRAM accessible by Processor '1' and the slave expansion port.

• Global Memory

Either 128K x 32 0ws SRAM, expandable to 512K x 32 or 1M x 32 3ws DRAM, expandable to 4M x 32.

• Expansion Ports

Master: 32-bit bidirectional 16.67 MHz expansion bus mapped into Processor 0's secondary address space and accessible via a 50 way IDC male connector (ribbon cable).

Slave: 32-bit bidirectional 16.67 MHz access port connected to bank 1 of on-board DPRAM. Directly compatible with the master expansion port of another board and accessible via a 50 way IDC female connector (ribbon cable).

DSP~LINK: 16-bit parallel expansion connector for interfacing to peripheral I/O boards. Supports transfer rates up to 3.33M 16 bit words/second via a 50 way IDC connector (ribbon cable).

• Serial Ports

Two synchronous 8.33 Mbps serial ports.
8, 16, 24, or 32-bit data frames.
Software configurable.
DB15 connector.

• Analog Interface (optional)

Dual 18-bit A/D and D/A converters.

108 dB dynamic range.

Better than 90 dB signal/noise.

THD + noise < 0.005 dB.

200 KHz maximum sample rate triggered by on-board timers or an external trigger.

Burr Brown SH5537 S/H circuit on each input.

4th order input and output Butterworth filters, resistor programmable and bypassable.

• VMEbus Interface

VMEbus A32 D32 slave interface.

VMEbus specification rev C1 compatible.

D16,D08(E0),BLT transfers also supported.

Occupies 2 Mwords in VME memory space.

VMEbus interruptible by either processor via STSTATUS/ID vector.

Either processor interruptible from the VMEbus via control registers.

• Physical

Standard 6U double Eurocard.

• Electrical

Maximum power 25 W.

Operating temperature 10 to 50 deg C.

Storage temperature -20 to +85 deg C.

Humidity 90% (non-condensing).

Versatile Array Signal Processor (VASP)

Product Line Overview

Advance Information



Pictured above is the Two-Port Memory Board (left) and the Input /Output Processor Board. Missing is the General Signal Processor Board.

FEATURES

- Array Signal Processing capability based on the Motorola DSP96002 processing element.
- Modular Three Board Set with 6U FutureBus+ Form Factor.
- A "building block" architecture which allows the VASP array processing system to be designed to fit the processing requirements of a specific application.
- Unlimited architecture topologies are possible, including conventional array processing structures such as:
 - Systolic Arrays Cubic Structures
 - Linear Pipelines Ring Networks
- A typical configuration performance of:
 - Peak Throughput capability of over 2.2 GFLOPS
 - 4.0 Gbits/sec Internal Data Bandwidth
 - 320 Mbits/sec Input/Output Data Rates
 - 100 Mbytes Memory Capacity

(based on a 20 slot chassis with five processing stages)

Applications of the VASP technology include military and commercial real-time high speed array processors for:

- radar
- sonar
- ECM, ECCM
- video imaging
- remote sensing
- pattern recognition
- medical imaging
- ray tracing

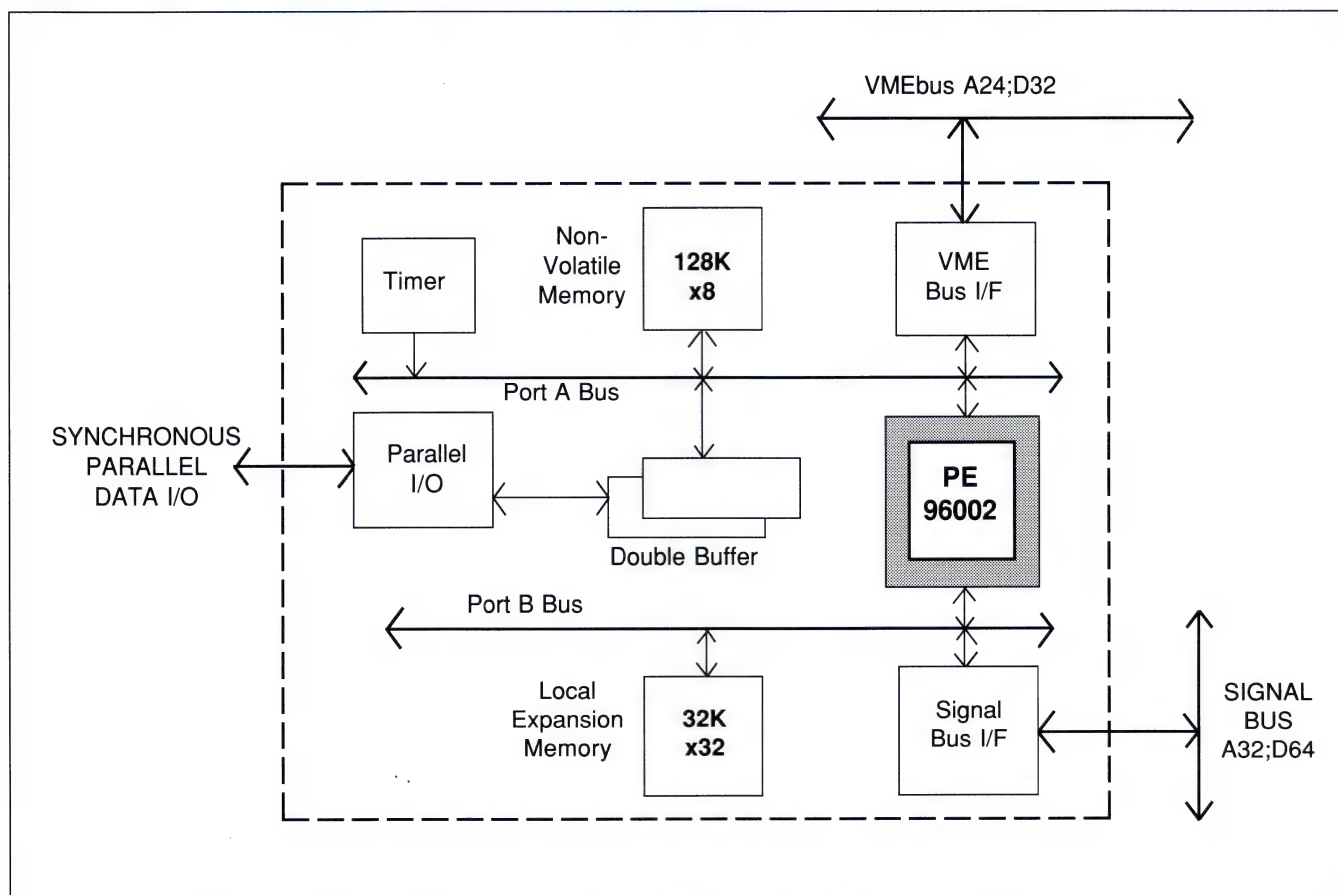
PRODUCT DESCRIPTION

The VASP architecture building blocks consist of the:

- Input/Output Processor Board
- General Signal Processor Board
- Two-Port Memory Board

Optimized for DSP applications, the VASP uses an array pipelining technique to achieve real time throughput. A high bandwidth proprietary signal bus along with pipeline memories facilitate array data transfers between the signal processing stages. At each stage, massive parallelism of processing elements is permitted to provide the required resources for algorithm execution.

The proprietary signal bus is the primary mechanism for transporting data in the system and has a bandwidth of 100 Mbytes/second. Several independent signal buses are permitted (nominally one per stage), providing excellent data transport capabilities. An industry standard VME bus interface is also provided for executive control and optional data input/output.



The Input/Output Processor Board is optimized for supplying data to and/or retrieving data from the VASP array processing system. The Input/Output Processor Board may also be configured as a standalone, DSP96002 based, digital signal processing VME board.

In addition to the Motorola DSP96002 processing element, the Input/Output Processor Board includes three independent bidirectional data interfaces:

- parallel input/output interface
- VME bus interface
- signal bus interface

The parallel input/output interface supports data exchange with external sensors or devices. A FIFO memory connects the parallel interface to the Motorola DSP96002 processing element.

The VME bus interface provides high bandwidth data transfers between the resident DSP96002 and any device on the VME bus.

The signal bus interface allows very high speed bidirectional

data transfers between the Motorola DSP96002 and other devices on the proprietary signal bus.

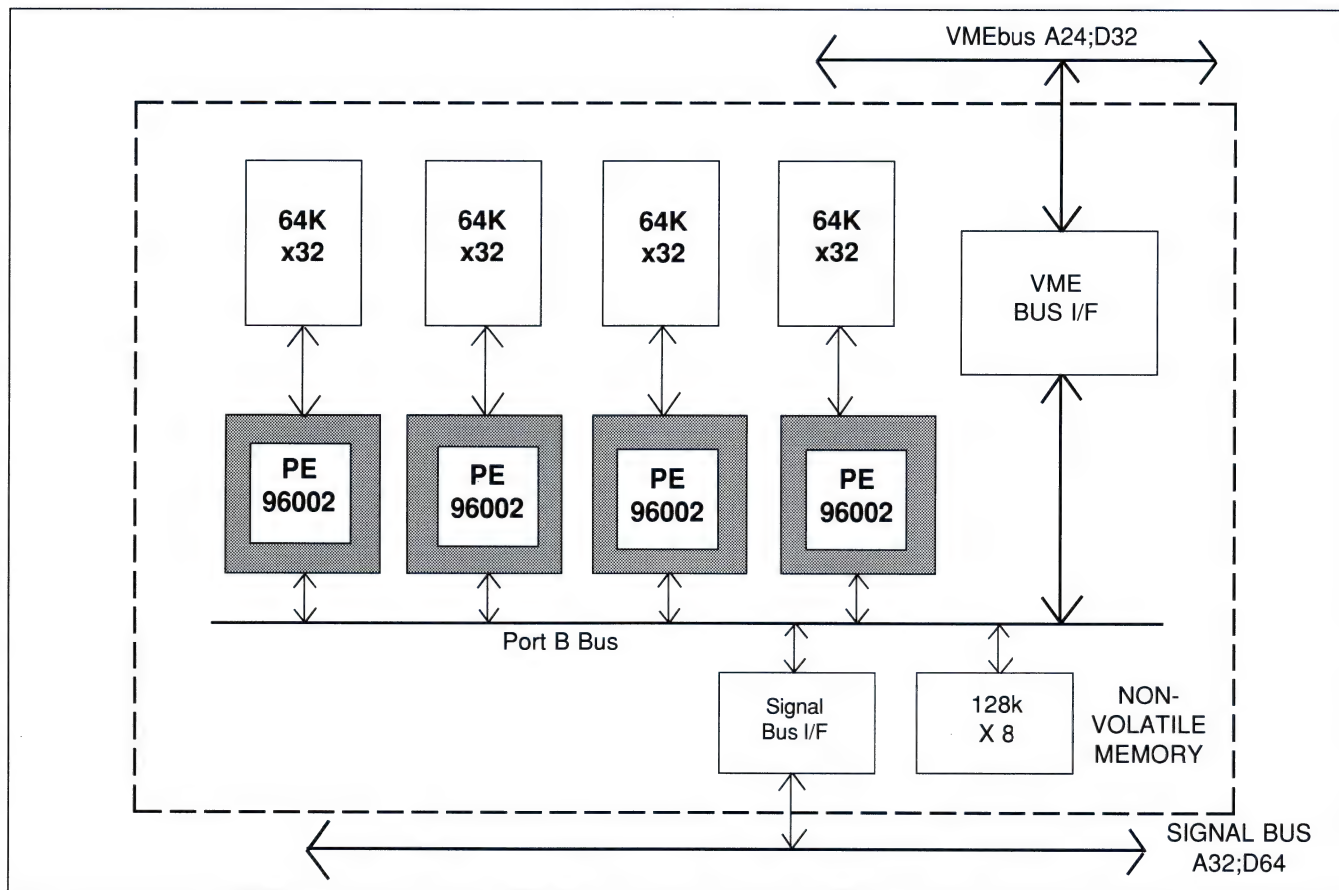
SPECIFICATIONS

Processing element:	Motorola DSP96002
Local Memory	32K x 32
Peak Throughput	40 MFLOPS

Parallel Data Interface:	
Input Only	32-bits
Output Only	32-bits
Bidirectional	16-bits input/16-bits output
Data Rate	10 MHz (maximum)

VME Bus Interface:	
Address	24-bits
Data	32-bits
Transfer Rate	10 Mbytes/sec

Signal Bus Interface:	
Address	32-bits
Data	64-bits
Transfer Rate	25 Mbytes/sec (DMA) 50 Mbytes/sec (programmed I/O)



The General Signal Processor (GSP) Board is optimized for data and signal processing. Four Motorola DSP96002 processing elements (PEs) are included on each GSP Board. Multiple GSP boards can be combined to provide the required array processing power for a specific application.

The operation of each PE involves three primary functions:

- acquisition of input data from external memory to local PE memory
- processing of data within local memory
- output of processed data to external memory space

The input and output tasks are normally overlapped with data processing and therefore do not degrade the computing resources of the PE. The processing from local memory releases a particular PE from the global bus and permits the connection of multiple GSP boards to a common bus.

A VME bus interface is provided to each DSP96002 processing element for executive control, data exchange, and status monitoring.

SPECIFICATIONS

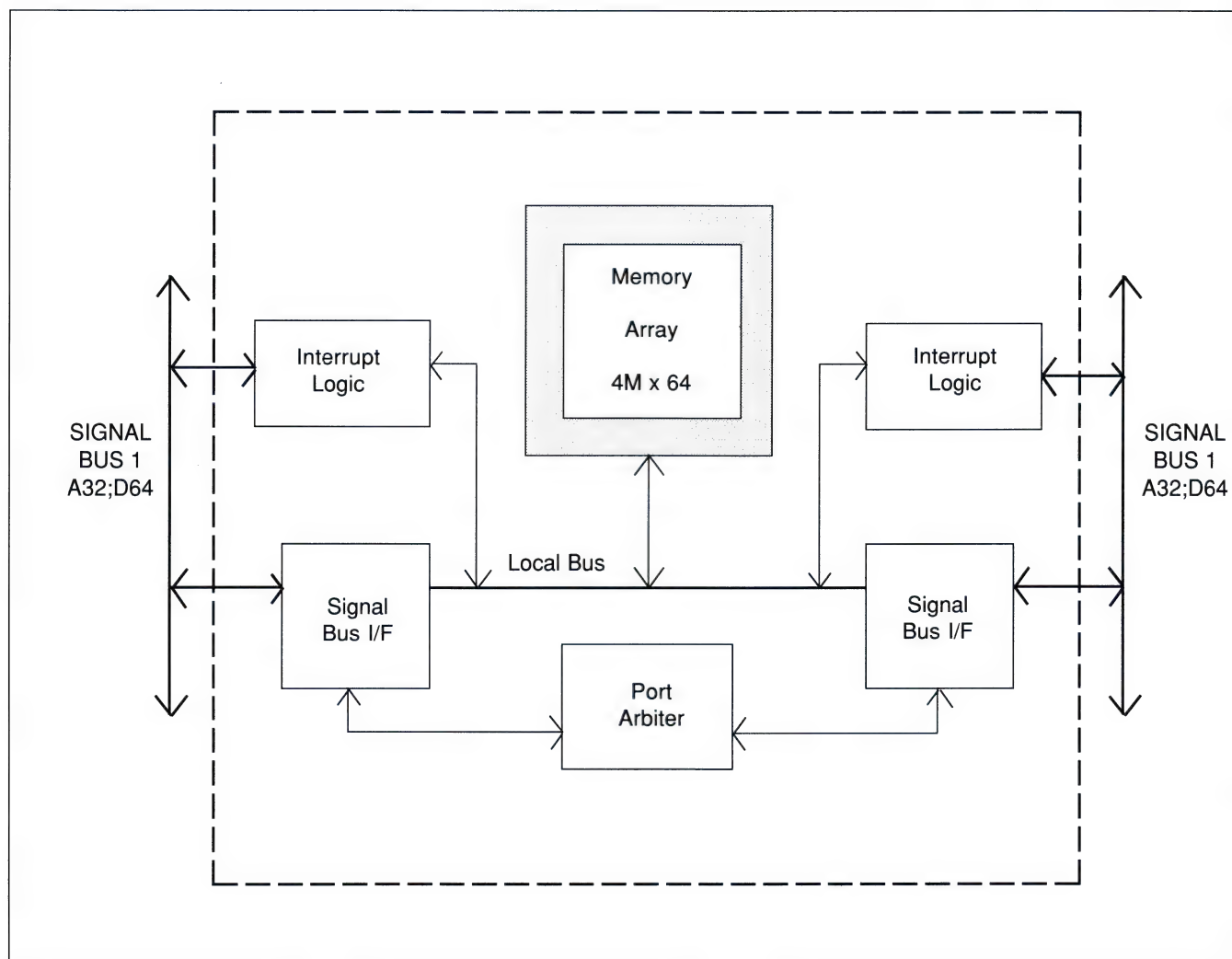
Number of processing elements 4

Processing Element: Motorola DSP96002
Expansion Memory 64K x 32
Peak Throughput 40 MFLOPS
Total Peak Throughput 160 MFLOPS

Signal Bus:
Data 64-bits
Address 32-bits
Data Transfer* 25 Mbytes/sec (DMA)
50 Mbytes/sec (programmed I/O)

* Per GSP to a maximum of 100 Mbytes/sec

VME Bus:
Slave Address 24 bits
Data 32 bits



The Two-Port Memory Board is the primary mechanism for connecting successive signal processing stages. Each port of the memory connects to a unique signal bus and allows simultaneous full read/write access. The memory is mapped onto both signal buses as 4M x 64 bits and supports efficient storage of 8, 12, 16, 24, 32, 48, and 64 bit data. The Two-Port Memory Board can be used for data buffers, interprocessor communications, configuration data and intermediate data. Multiple memory boards can be paralleled to support larger buffer sizes.

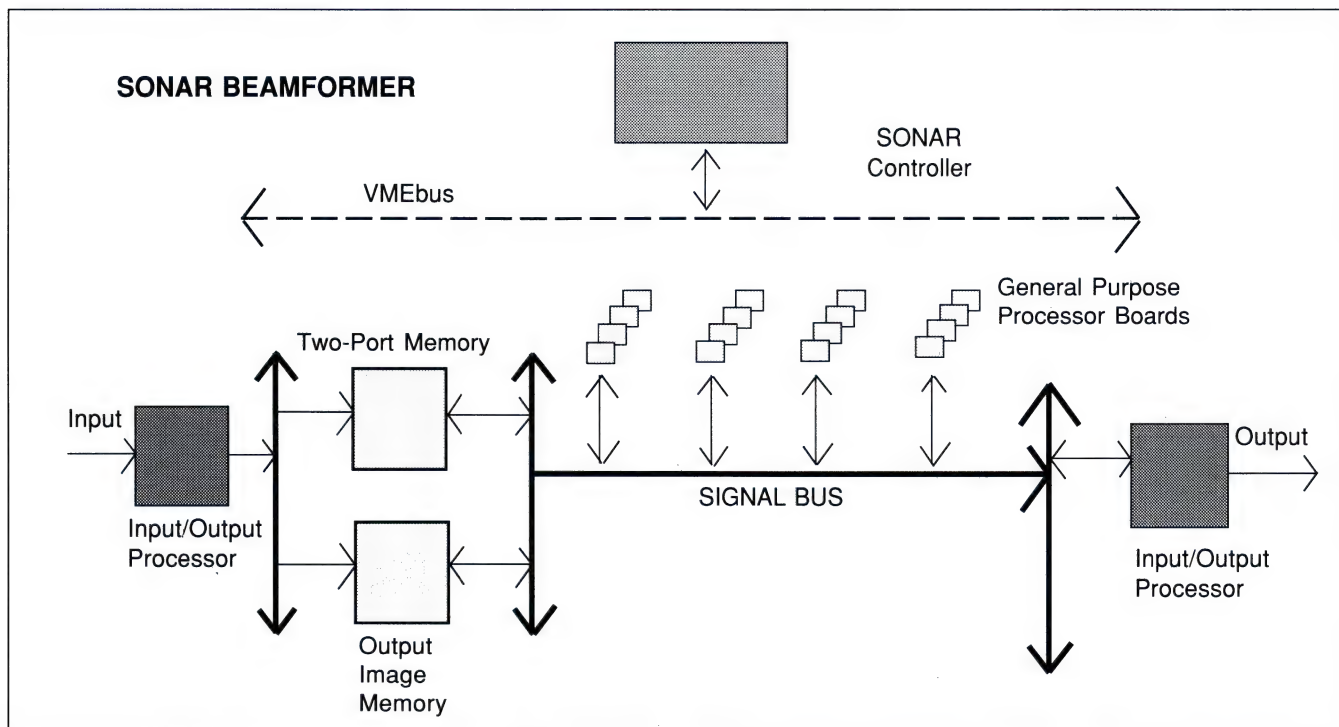
Also contained on each Two-Port Memory Board is an interrupt (data available) register used by a signal processing stage to notify the successor or predecessor stage that data is available, supporting "data driven" and other interlocking mechanisms.

SPECIFICATIONS

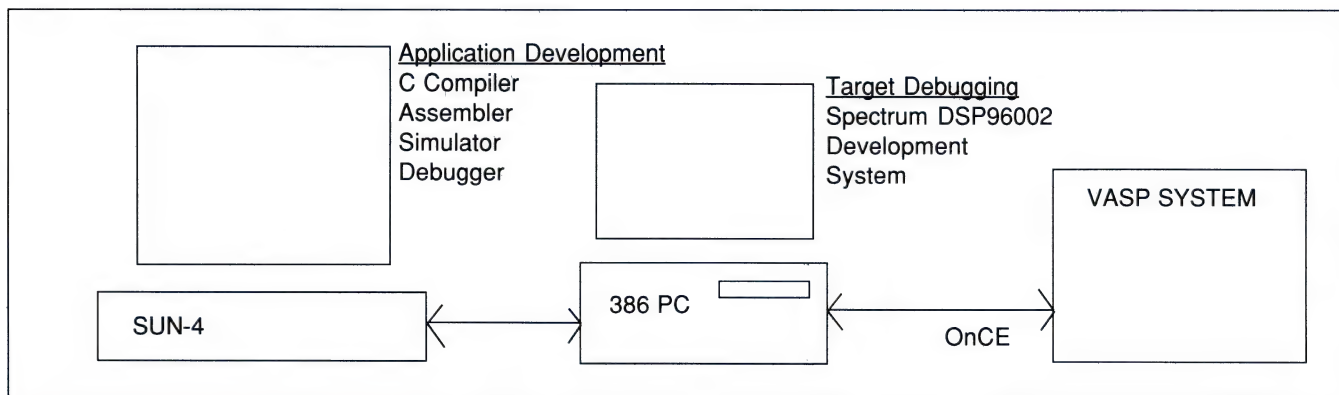
Memory Size	32 Mbytes
Organization	4M x 64
Access Time	75 ns per port

Application Example

VASP Architecture



Development Environment



VASP DEVELOPMENT ENVIRONMENT

For each VASP application, two software components must be developed: the execute control software, and the processing element application firmware. The executive controller is a VME based single board computer for which a mature development environment exists for C, Pascal, and ADA languages.

The primary platform for PE application firmware development is a SUN-3 or SUN-4 workstation with the following tools:

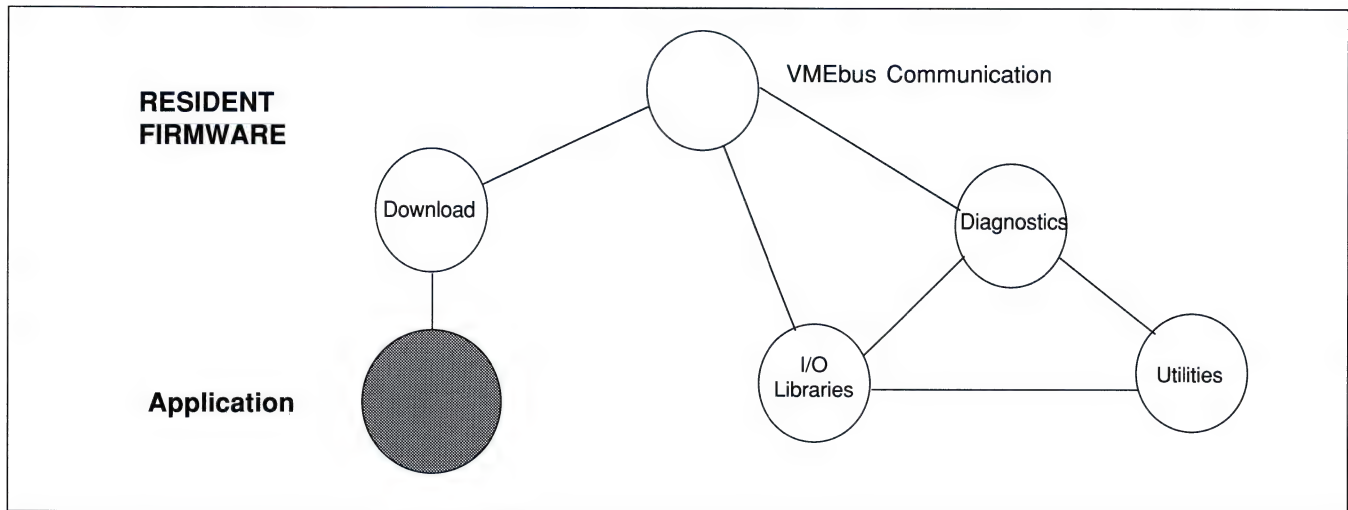
- Motorola 96002 Assembler, Simulator, and DSP Application Library
- Intermetrics 96002 C Compiler and Debugger

- Comdisco Signal Processing Workstation (SPW), a CASE tool for DSP algorithm simulation, debugging, and code generation

Code for the PE application firmware may be generated in C or assembler and debugged on an IBM AT/386 using Spectrum's DSP96002 Development System and the OnCE interface. MacDonald Dettwiler, the developer and supplier of the VASP resident firmware, is available to provide consulting services in this area.

Resident Firmware

VASP Architecture



RESIDENT FIRMWARE

Each Motorola DSP96002 processing element (PE) contains resident firmware for performing the following functions:

- initialization
- VME bus control and communication
- diagnostic procedures
- configuration of on-board resources
- data transfers between the PE and the various interfaces
- application program downloading
- allocate, de-allocate
- peek, poke
- get, put
- load, execute, abort
- show status, dump stack, re-boot

On power-up the resident firmware is automatically loaded and executed by the PE. All hardware resources are tested with resident diagnostic routines and a status indication provided. The PE then enters an idle state waiting for commands or application programs from an executive controller (VME bus). Optionally, the PEs may be configured to load and execute an application program which resides in the non-volatile memory. The application program assumes complete control over the PE and may overlay the resident firmware or use the functionality as provided.

The resident firmware makes each PE appear as a device to the executive controller. The following standard commands are provided for PE control and communication from the VME bus:

The peek and poke commands use programmed I/O control for accessing the various PE interfaces whereas the get and put commands use the on-chip DMA controller.

Several utilities are provided for configuring the on-board hardware resources. These utilities are accessed by the executive controller commands and are available to the application, thus insulating the developer from the low-level hardware details. The utilities include:

- timer control
- signal bus control
- two-port memory control
- interface control

Routines for DMA and programmed I/O transfers between a PE and the various interfaces are provided in the input output libraries.

Software Development Tools

Spectrum offers software development tools that address DSP chip code development, PC code development, and data analysis and filter design.

DSP chip code development tools include Assemblers, Simulators, and 'C' Compilers from the chip manufacturers, as well as debug monitors which are included with each System or Processor Board.

PC code development tools include a High-Level Language Library of board interface functions (object loader, data transfer, initialization, and hardware control) for which 'C' and Assembly Language source code is included as well as examples of how to use the functions. Microsoft-compatible object code is also included for compatibility with other Microsoft languages. These libraries are included with each System or Processor Board.

Data Analysis and Filter Design software includes standalone PC packages such as DISPRO Filter Design, and packages that are integrated with certain SPECTRUM boards such as Hypersignal Workstation and Momentum Filter Design.

DSP Chip Development Tools from Third Parties

Texas Instruments

TMS320C25 Macro Assembler/Linker.
TMS320C25 'C' Compiler.
TMS320C30 Macro Assembler/Linker.
TMS320C30 'C' Compiler.

Motorola

DSP56001CLASx Assembler, Linker/Librarian & Simulator.
DSP56KCCx 'C' Language Compiler.
DSP96002CLASx Assembler, Linker/Librarian & Simulator.
DSP96KCCx 'C' Language Compiler.

Analog Devices

ADSP-2100 Cross-Software and Simulator.
ADSP-2100 'C' Compiler.
ADSP-2101 Cross Software and Simulator.
ADSP-2101 'C' Compiler.

AT&T

DSP32C Assembler/Linker and Simulator.
DSP32C 'C' Compiler.
DSP32C Applications Library.

Loughborough Sound Images

TMS320C25 'C' Compiler

Spectron Microsystems

SPOX™ Real-Time Operating System for the TMS320C30.
SPOX™ Real-Time Operating System for the DSP96002.

Intermetrics

DSP96002 Assembler
DSP96002 'C' Compiler.

LSI 'C' Compiler

The LSI 'C' Compiler from Loughborough Sound Images (LSI) is a complete MS-DOS/PC-DOS facility for writing DSP software in 'C' programming language and for compiling that software into executable TMS320C25 object code. This code will run directly on the C25 processor.

When used with the TMS320C25 System or Processor Boards, the 'C' Compiler provides a new level of application development support. The LSI 'C' Compiler allows users to write programs without knowledge of assembly language programming and to use high-level code in the final system.

The 'C' Compiler is an excellent tool for software developers who are comfortable with assembly language but are seeking greater speed in developing DSP software. All code can initially be written in 'C' for proof-of-concept, and later optimized by writing 'C'-callable assembly language functions for speed-critical code. Further, the assembly language code produced by the 'C' Compiler can be "tweaked" by hand. The software development cycle can be further accelerated since previously developed algorithms written in 'C' can be recompiled and executed.

The TMS320C25 System or Processor Board are highly recommended since the examples in the manual make fre-

quent references to these systems. The LSI 'C' Compiler run-time start-up code sets the program/data memory sizes, stack location, program load addresses, and other configurable parameters to default to those necessary for either of these boards. These parameters can be altered to function with any C25 hardware setup or monitor program.

FEATURES

- Preprocessor and Linking Assembler included.
- Full integer implementation of 'C' as defined by K&R ('float' and 'double' types are not supported).
- Supports all integer data types including 'long' and 'unsigned'.
- Functions are included to read/write C25 I/O ports.
- Interrupts are handled using the standard 'C' 'signal' function.
- Includes source code for run-time start-up code, interrupt-handling library, I/O library, and double precision division/multiplication library.
- Speed critical code can be written in assembly language, called as functions from 'C', and linked in with the Linking Assembler.
- Five auxiliary registers are available for use in assembly language subroutines.
- Programs can be written for systems containing RAM, EPROM, or both.
- Outputs object code in Texas Instruments 'TAG' format.

TMS320C1x Development System for the IBM-PC

(C1x) Part Number: 600-00392
(EPROM) Part Number: 600-00400



The TMS320C1x Development System provides a complete development environment for any of Texas Instruments' first-generation TMS320C1x single-chip DSPs. The Development System consists of a Software Development System (SDS) and optional hardware modules including an EPROM Programmer Module and full in-circuit emulator (ICE) Modules. This is the first system to support Texas Instruments' new TMS320C14 DSP microcontroller, as well as supporting the TMS320C10, -C15, -C17 and their EPROM equivalents.

FEATURES

Software Development System (SDS)

- Window-based monitor/debugger software includes single step, breakpoint and file I/O.
- Simulation of all members of TMS320C1x family.
- LSI TMS320C1x Absolute Assembler and a text editor.
- IBM-PC/XT/AT or true compatible plug-in card.

Optional Hardware Modules

- EPROM Programmer Module for the TMS320E15, -E17 and -E14 processors.
- Full-featured in-circuit emulator/trace modules.

The TMS320C1x Development System provides an effective, low-cost entry to real-time development and satisfies a wide range of objectives, from processor evaluation and software development/debugging to full-speed emulation and trace capture in target hardware. Sample applications that take full advantage of the concurrent emulation and trace capture operations are: developing a speech coder on the TMS320C10, evaluating the TMS320C15 as a digital filter/modem in a mobile radio, or developing an AC motor drive strategy on the TMS320C14.

SOFTWARE DEVELOPMENT SYSTEM (SDS)

The SDS is a complete software development environment that includes a full-featured monitor/debugger, assembler, and PC plug-in card for full speed execution. The SDS can be configured to simulate the different members of the TMS320C1x family simply by changing the I/O files. The software development environment is unchanged, as all these processors are source and object code compatible.

The color window-based monitor/debugger allows program and data downloading, full-speed execution, single step, breakpoint with event counter, state save, file I/O and DOS function access. The three windows are: Disassembled Program Memory, Data Memory, and Register Dump. All commands are assigned to Function keys with a transparent pop-up Command menu.

The LSI TMS320C1x Absolute Assembler and text editor are included with the package. SDS can be configured to invoke any assembler or editor/word processor from the menu.

The PC plug-in card provides all the resources for software development and allows full-speed code execution. Since the SDS does not reserve any memory or register locations, all chip resources are available to users. The card supports all C1x processors with full external memory. I/O operations are simulated via file transfers to and from the PC. A programmable hardware breakpoint register allows full-speed execution to a breakpoint. The 8-bit event counter allows up to 256 occurrences of the breakpoint before halting the program.

EPROM PROGRAMMER MODULE

For fast prototyping and algorithm proving in stand-alone target systems, users may program EPROM variants of the TMS320C1x processors by connecting the Programmer Module to the PC plug-in card via ribbon cable. The Module includes sockets for TMS320E15 and -E17 (40-pin) and for the -E14 (68-pin). There is an on-board Vpp generator. The Module is directly controlled from the SDS and software is included for programming TMS320E1x parts.

SPECIFICATIONS (Electrical/Physical)

SDS PC Interface Board

Dimensions: 13.4"L x 4.5" H x .7" D, full length PC card.
Connections: 37 pin D-Type connector interfaces to EPROM programmer or ICE Module via ribbon cable.
Power Consumption: +5V @ 1.5A

EPROM Programmer

Dimensions: 10" x 4", stand-alone PCB.
Connections: 37 pin D-Type connector interfaces to SDS PC Interface Board via 37 pin ribbon cable.
Power Consumption: +5V @ 250mA, +12V @ 50mA, via SDS PC Interface.

The TMS320C14/E14 In-Circuit Emulator is a stand-alone unit designed to be used in conjunction with Spectrum's TMS320C1x Development System. The ICE provides extensive hardware debug and development support for the C14 or E14, complementing the software development support provided by the Development System. Programs are generated and assembled on the PC under DOS and then downloaded either to the SDS PC card, or to the ICE Module via a ribbon cable which interfaces the two.

EMULATION

Emulation and trace functions are available from the ICE module when it is connected to the PC card interface and enabled via the SDS10 debug monitor.

The ICE module provides full speed functional emulation of the TMS320C14 including I/O peripherals and registers, across all operating frequencies up to the device's current maximum of 25.6 MHz. An on-board oscillator acts as an internal clock source for the emulator. An option is also provided to enable an external clock to drive the emulator from the target system.

The TMS320C14's microprocessor and microcomputer modes are both supported. Internal memory is emulated by 4k words of on-board fast SRAM into which programs can be downloaded, executed and debugged. In microprocessor mode the emulator will access the user's target memory. The TMS320C14 has a software feature which enables the user to dynamically switch between microprocessor and microcomputer modes of operation. This feature is fully emulated by the ICE module.

Physical emulation of the TMS320C14/E14 in the target is performed by the emulation probe which consists of 4 short ribbon cable connectors terminating in a header with a 68 pin PLCC footprint.

BREAKPOINT SYSTEM

One hardware breakpoint can be specified and enabled at any one time. This breakpoint can be configured to detect an access to either a program memory address or to one of the TMS320C14's I/O peripherals or registers. An 8 bit event counter is provided allowing up to 255 breakpoint events before the breakpoint trigger is activated. The breakpoint can also be programmed to continue or halt program execution when the trigger becomes active. This important feature enables the trace buffer to be analyzed while the emulator is still running.

TRACE BUFFER

An 8K (8192) frame trace buffer is provided for keeping a history of actual instruction execution and I/O activity. The trace hardware captures and stores 72 signals on every clock cycle. These include address, data I/O and control signals and data from internal peripheral register accesses. The trace

operation is automatically enabled when the emulator begins program execution and will continue, wrapping around when buffer is full, until a breakpoint trigger occurs.

An 8 bit hardware delay counter then allows the trace to continue for up to 256 clock cycles beyond the trigger. When the trace has halted, the trace display may be activated through the debug monitor. The emulator can still be running at this time depending on whether or not the breakpoint was configured to halt program execution at the trigger. Search and scroll facilities are provided to analyze the display which includes disassembled program instructions. The ICE module is also equipped with a 32 bit counter/timer which is enabled during trace capture. This can be used to time stamp the breakpoint or measure algorithm execution time.

USER INTERFACE

All functions and commands for the ICE are initiated from within the SDS10 environment. This system runs on IBM PC/XT/AT's and true compatibles, with 640K bytes of RAM and either EGA or VGA graphics.

Features include loading and saving of programs, full speed execution, set/enable breakpoint with event count, modify registers memory and counters, on-line help, access trace display, load and save machine state, start up waveform utilities, EPROM DSP programmer functions and access to DOS commands including a quick edit/assemble/link/load sequence.

SPECIFICATIONS (Electrical/Physical)

Dimensions:

11"L x 11"W x 2.5"H, stand-alone casing.

Connections:

37 pin D-Type connector interfaces to SDS PC Interface Board via 37 pin ribbon cable.

Power Consumption:

+5V @ 2.5A, via PC Interface.

Emulation Probe:

Four 20 pin ribbon cables, terminating in a 68 pin PLCC pin-out.

Host Requirements:

IBM PC/XT/AT or true compatible with:

- 640K bytes RAM
- Hard disk
- EGA or VGA
- One 8-bit PC Bus slot available
- DOS 3.0 or later

Speech Workstation

(With Proc. Card) Part Number: 600-00923
(W/O Proc. Card) Part Number: 600-00932

The Speech Workstation is a unique product for the IBM PC/AT that integrates a 50 MHz TMS320C25 DSP plug-in board, 16-bit data acquisition, and a menu driven signal processing analysis package. The Speech Workstation offers a user-friendly environment for the capture, display, and analysis of audio signals. Display options include spectrograms, spectral slices, time waveform plots, energy calculations, fundamental frequency contours, and user generated signals.

DATA ACQUISITION

Two independent input channels from line or microphone sources may be sampled at rates up to 40 KHz/channel using 16-bit Motorola Sigma-Delta ADCs. These converters provide a linear phase digital anti-aliasing filter whose cutoff frequency automatically tracks the sample rate. Each input channel has a programmable gain amplifier and a software controlled pre-emphasis filter which together can provide the following responses:

- Flat
- 6dB/octave rise from 0 Hz
- Flat to 1 KHz and then rising at 6 db/Octave



Pull-Down Menu

The output channel can be connected directly to a speaker. The signal is low pass filtered and a volume control for the speaker is mounted on the back panel.

SIGNAL ANALYSIS

During analysis, the PC screen can be divided into five areas. The top area contains the title block and pull down menus. The bottom area contains the time domain representation of the input signal showing either the entire contents of the capture buffer or simply the section undergoing spectral analysis. The large center area displays the results of the spectral analysis. Two optional pop up areas can be used to display spectral slices, expanded time waveforms, or fundamental frequency contours.

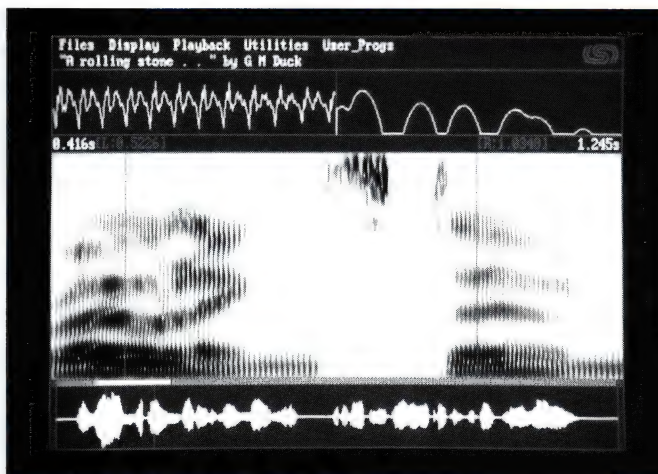
All system functions can be selected quickly and easily using a mouse. Pull down menus, dialog boxes and comprehensive on-line help screens present the user with a pleasant working

SPECTRUM Signal Processing Inc.

Eastern US: (508) 366-7355 or 800-323-1842

Western US: 800-663-8986

Canada: (604) 438-7266



Wideband Spectrogram & pop-ups (waveform & spectral slice)

environment. The Speech Workstation uses EGA or VGA graphics in 16 colors with a resolution of 640 x 350 or 640 x 480 respectively. Hardcopy outputs can be printed on a laser printer or in full color on certain ink jet printers.

SYSTEM REQUIREMENTS

- IBM PC/AT (286/386)
- 640K Bytes RAM
- Hard Disk (min. 20M Bytes)
- RAM Disk (for high speed sampling)
- DOS 3.0 or higher
- EGA/VGA monitor
- Microsoft mouse

DSP Processor Card:

TMS320C25-50 processor card with 64 Kwords.

Data Acquisition Card:

Two input channels with 2 Motorola DSP56ADC16 Sigma-Delta ADCs.

One output channel with Burr-Brown PCM56 DAC.

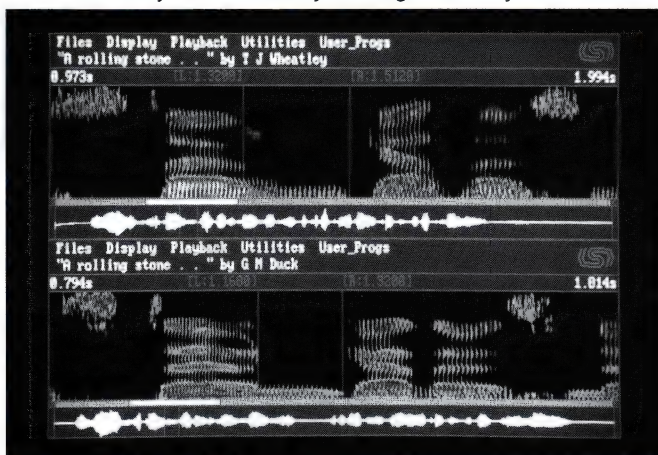
Sampling rates of 8, 10, 16, 20, 32, 40 KHz with external clock option.

Programmable gain amplifier and pre-emphasis filter on analog inputs.

Reconstruction filter on analog output.

Printer Support:

HP Laserjet II, HP Paintjet, Integrex Colorjet



Split Screen Mode (Horizontal)

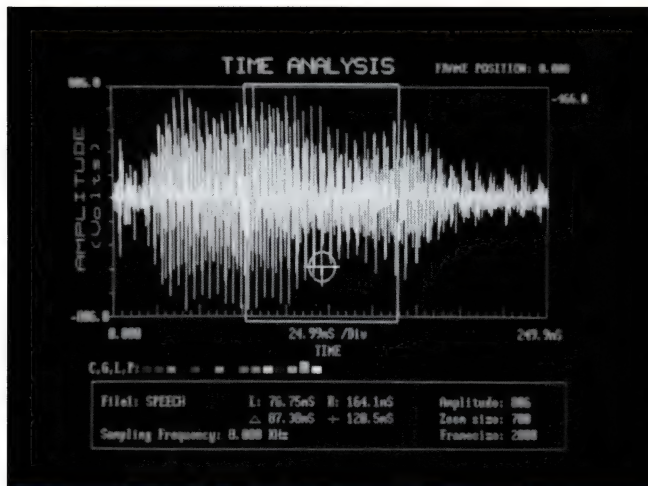
Hypersignal

Integrated Digital Signal Processing

(Hypersignal Workstation) Part Number: 100-00243
(Hypersignal-Plus) Part Number: 100-00441

The **Hypersignal-Plus** and **Hypersignal Workstation** software packages create and maintain an integrated digital signal processing environment that offers an efficient menu-driven human interface, super fast digital signal processing functions, automatic file management, automatic time/frequency data flow, excellent graphics and in the case of Hypersignal Workstation software, various real-time signal acquisition and processing functions.

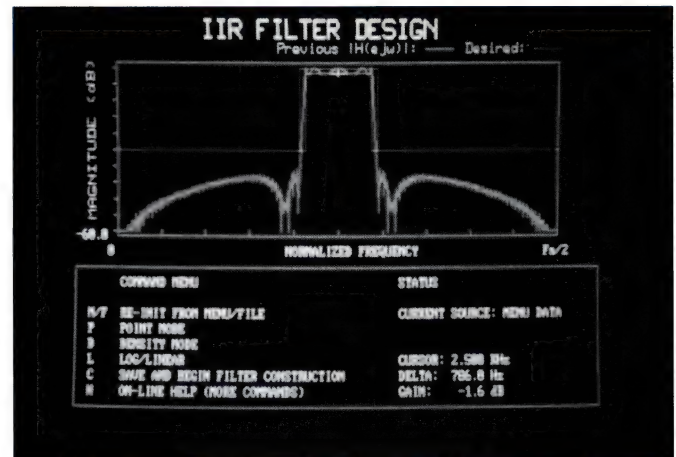
Inside this environment the user can, for example, guide sampled data from initial acquisition and display in the time domain, through built-in functions such as auto correlation and filtering, or user-arbitrary functions such as signal arithmetic, math functions, and signal calculus, to transformation and display in the frequency domain. Waveform data can be imported from disk files, serial ports, and PC memory in many ASCII and binary formats. Output file parameters support interleaved/ multiplexed data channels.



Time domain features include single or dual waveform displays, FFTs, FIR filter design and simulation (convolution), IIR filter design and simulation (recursive filtering), linear predictive coding (LPC) analysis up to 31st order, and recursive and non-recursive difference equations.

Frequency domain features include magnitude displays in log and amplitude-squared forms, phase displays wrapped and unwrapped, group delay displays, inverse FFTs, 3D spectrograms, 2D spectrographs, pole-zero analysis of IIR filter designs with s-plane and z-plane displays, and power spectra generation.

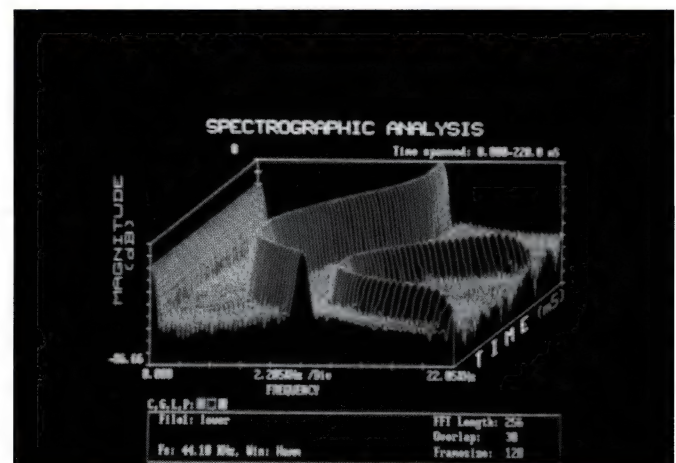
Hypersignal code generation for FIR and IIR filters can produce C or assembler code for Texas Instruments TMS320xx, AT&T DSPxx, Motorola DSP5600x, and Analog Devices ADSP-210x digital signal processing ICs. Coefficient base address, quantization and rounding, and IIR cascade structure (all pole, mixed pole-zero, direct-form) can be user selected.



Over 200 screens of context dependent, on-line help is available. User options include mouse interface, extensive graphics display selection, and hardcopy output. Frame-based analysis has full zoom and pan capability in both time and frequency domains. Also, an "undo" function is offered. An environment save file maintains all display parameters, function parameters and selections, menu states, and data fields between Hypersignal sessions.

Hypersignal Workstation includes all of the above features and offers a number of real time signal acquisition and accelerated processing features which are fully supported by Spectrum Signal Processing's TMS320C25, TMS320C30, DSP56001, DSP32C, ADSP-2100 series System Boards.

Hypersignal Workstation can utilize the power of the DSP processor to accelerate the calculation of FFTs and inverse FFTs. Continuous A/D acquisition or D/A generation at rates up to 150 KHz with a RAM disk and 110 KHz with a hard disk are possible. In addition, Hypersignal Workstation can function as a digital oscilloscope and real-time spectrum analyzer.



Data Analysis and Filter Design Software

DADISP

Data Analysis & Digital Signal Processing

DADiSP Version 1.05 is a post acquisition, data analysis software program based on the principle of a spreadsheet. Unlike typical analysis programs or spreadsheets, DADiSP is a graphics-based worksheet allowing you to display and manipulate up to 64 waveforms at once or create a data reduction chain containing up to 64 windows of complex processing steps.

Single or multi channel signals of any length can be imported as ASCII or Binary files from disk. Once loaded into DADiSP, these signals are stored within a database organized into Labbooks, Datasets, and Worksheets.

DADiSP supplies more than 160 functions to transform data including signal arithmetic, signal calculus, waveform generation, Fourier analysis, FFTs, correlations, trigonometric, and statistical routines. These functions can be used separately or combined in a single expression, or as part of a user defined Macro. Complex numbers and engineering unit conversions are also supported. A full set of "G" functions lets you generate any type of waveform ranging from a sine wave to a complex random signal.

Any Worksheet signal can be zoomed to full screen size,

scrolled, expanded, compressed, cursored, and edited. You can also add grids, change scales, and send any window to a printer or plotter, with or without background signal information. Also, any number of signals can be overlaid within a window.

The DSP pipeline feature allows ASCII or Binary files to be read or written directly from within a Worksheet. The pipeline lets you run external software such as data acquisition, signal filtering, and pen-plotting without leaving the Worksheet.

DADiSP Version 2.0 adds: new analysis functions; the ability to create customized menus for specific applications; a broader range of graphics options; the ability to accept tabular data; automatic reports that provide descriptive and background information on any graphic window; free-form annotation with text and line-drawing; and control features to enable DADiSP to monitor control equipment and processes.

Version 2.0 requires 2 Mbytes of extended memory but leaves 400 Kbytes of main memory free for other programs to use. The new analysis functions allow each window's display format to be changed to bar chart, symbol plot, scatter plot, 3D surface (waterfall) chart, histogram or data table. Also, X-Y plots are now supported.

MOMENTUM

Filter Design and Analysis System

Momentum's Filter Design and Analysis System is available in two versions for the IBM-PC. Version 1 features IIR and FIR designs as well as a unique system analysis capability allowing determination of the characteristics of a given transfer function.

Version 2 is a superset of Version 1 and incorporates advanced design features such as Phase Equalization, Hilbert Transformer and Arbitrary Magnitude Filters, Filter compensation features, logarithmic frequency scale option, digitization of s-domain transfer functions, and significantly increased filter lengths.

These systems are characterized by outstanding graphics, ease of use and exceptionally high performance. Help screens are available for most data fields enabling the unsophisticated user to make effective use of the system. Additional features include menu-driven screens, coefficient quantization from 8 to 32 bits, filter specification retention, all design calculations performed in 64-bit floating point arithmetic and easy to read documentation. A wide variety of output devices are supported.

The Filter Design and Analysis System also includes a code generator which directly supports Spectrum's DSP56001 System Board.

DISPRO®

Digital Filter Design and Evaluation

DISPRO is an IBM-PC compatible program that easily produces coefficients for FIR and IIR digital filters and provides tools for filter performance analysis.

Users can interactively optimize tradeoffs between edge frequencies, ripple size, and number of stages to make filters come close to design specifications on the first iteration.

IIR types (to order 30) include Butterworth, Chebyshev I and II, and Elliptic.

FIR types include Parks-McClellan-Remez to length 430, and Kaiser window to length 1023. Arbitrary magnitude and $\sin(x)/x$ compensation are supported.

Coefficients (2 to 24 bits fixed point or 32 bit floating point) are output to disk files in generic format or in one of several DSP assembly language source formats. Frequency or time domain response data for any coefficient length can be graphed or sent to a disk file (filter stimulus can be generated by the user or within DISPRO).

The comprehensive User Manual includes tutorial information to aid selection of filter types.

DISPRO is a registered trademark of Signix Corporation.

PC SYSTEM BOARDS

	PART NO.	PRICE
TMS320C25 System Board (40 MHz Version)	600-00103	\$ 1,995.00
RAM upgrade - 0 wait state (35ns)		
Each 32K x 16 increment	202-00079	Please call
Maximum upgrade is 4 increments (128K x 16)		
50 MHz Upgrade for purchasers of P/N 600-00103 with S/N > 1000	700-00009	Please call
TMS320C25 System Board (50 MHz Version)	600-00734	\$ 2,150.00
RAM upgrades - 0 wait state (25ns)		
Each 32K x 16 increment	202-00079	Please call
Maximum upgrade is 4 increments (128K x 16)		
TMS320C50 System Board	600-01056	Please call
TMS320C30 System Board (with SPOX Run-Time Licence)	600-00554	\$ 4,795.00
RAM upgrade - 0 wait state (25ns)		
Each 64K x 32 increment	202-00189	Please call
Maximum upgrade is 2 additional increments		
TMS320C30 Real-Time System	600-00545	\$ 6,995.00
Includes TMS320C30 System Board with Assembler/Linker, C Compiler, and SPOX Operating System		
Memory Expansion Daughter Board:	600-00905	\$ 2,495.00
Includes 1M x 32 RAM - 3 wait state (80ns)		
Each additional 1M x 32 increment	202-00268	Please call
Maximum upgrade is 3 additional increments		
DSP56001 System Board	600-00202	\$ 2,995.00
RAM upgrades - 0 wait state (35ns)		
Each 64K x 24 increment	202-00105	Please call
Maximum upgrade is 3 increments (192K x 24)		
DSP56116 System Board	600-01101	Please call
DSP96002 System Board	600-00993	\$ 5,695.00
System Board with Motorola Assembler, Linker/Librarian, Simulator, and C Compiler	600-01074	\$ 6,895.00
System Board with Intermetrics Assembler, C Compiler, and SPOX	600-01083	\$ 8,095.00
Multiprocessing package with 4 System Boards (200 MFLOPS)	600-01092	\$19,495.00
Multi-processing Backplane	600-01128	\$ 315.00
ADSP-2100 System Board	600-00167	\$ 2,495.00
32 Kword program RAM upgrade - 0 wait state (30ns)	202-00088	Please call
System Board with Cross-Software and Simulator	600-00176	\$ 2,995.00
System Board with Cross-Software, Simulator and C Compiler	600-00301	\$ 3,995.00
C Compiler upgrade for purchasers of P/N 600-00176 above	100-00500	\$ 1,000.00
ADSP-2101 System Board	600-00671	\$ 1,995.00
14Kx24 program and 12Kx16 data RAM upgrade - 0 wait state (30ns)	202-00088	Please call
System Board with Cross-Software and Simulator	600-00914	\$ 2,395.00
System Board with Cross-Software, Simulator and C Compiler	600-00941	\$ 3,595.00
C Compiler upgrade for purchasers of P/N 600-00914 above	100-00509	\$ 1,200.00
DSP32C System Board	600-00455	\$ 2,995.00
128K x 32 RAM upgrade - 2 wait state (55ns)	202-00178	Please call
DSP32C Telephony Board	600-00851	\$ 2,495.00
128K x 32 RAM upgrade - 2 wait state (55ns)	202-00178	Please call
PDSP16488 Imaging/Graphics Board	606-00879	\$ 3,295.00
No RAM upgrades possible		

PC PROCESSOR BOARDS

TMS320C25 Data Acquisition Processor	600-00626	\$ 2,495.00
Processor Memory RAM upgrade - 0 wait state (35ns)		
128K x 16 SIMM replacement	202-00286	Please call
Buffer Memory upgrade - 1 wait state (120ns)		
Each 256K x 16 SIMM	202-00213	Please call
Maximum upgrade is 7 additional SIMMs		
TMS320C25 Processor Board (40 MHz Version)	600-00266	\$ 995.00
RAM upgrade - 0 wait state (45ns)		
Each 32K x 16 increment	202-00123	Please call
Maximum upgrade is 2 increments (64K x 16)		
50 MHz Upgrade for purchasers of P/N 600-00266 with S/N > 1000	700-00009	Please call
TMS320C25 Processor Board (50 MHz Version)	600-00653	\$ 1,150.00
RAM upgrade - 0 wait state (35ns)		
Each 32k x 16 increment	202-00079	Please call
Maximum upgrade is 2 increments (64K x 16)		
TMS320C30 Processor Board (with SPOX Run-Time Licence)	600-01011	\$ 3,795.00
RAM upgrade - 0 wait state (25ns)	202-00189	Please call
Processor Board with Assembler/Linker, C Compiler and SPOX Operating System	600-01110	\$ 5,995.00
DSP56001 Processor Board (20 MHz Version)	600-00211	\$ 1,495.00
RAM Upgrade - 0 wait state (35ns)		
Each 64K x 24 increment	202-00105	Please call
Maximum upgrade is 3 increments (192k x 24)		
DSP56001 Processor Board (27 MHz Version)	600-01065	\$ 1,695.00
Dual DSP56001 Processor Board	600-00752	\$ 2,995.00
Dual Channel Analog I/O Module	600-00761	\$ 1,395.00
Adaptive FIR Filter Module	600-00770	\$ 1,795.00
DSP~LINK Interface Module	600-00789	\$ 145.00
Digital Audio (AES/EBU) Receiver Module	600-01119	\$ 395.00
Memory Expansion Module	600-00957	\$ 895.00
Combination Memory Expansion & Digital Audio Module	600-00948	\$ 1,255.00
DSP32C Processor Board	600-00662	\$ 1,995.00
128K x 32 RAM upgrade - 2 wait state (55ns)	202-00178	Please call

DSP~LINK PERIPHERALS

4 Channel Analog I/O Board	600-00185	\$ 845.00
32 Channel Analog Input Board	600-00257	\$ 845.00
16 Channel Analog Output Board	600-00428	\$ 845.00
16-Bit Stereo Board	600-00491	\$ 1,195.00
Transient Capture Board	600-00464	\$ 1,195.00
4K x 8 FIFO upgrade - 35ns	202-00204	Please call
Pro-Audio (Basic)	600-00310	\$ 1,250.00
Pro-Audio Board (Extended with SONY PCM and MIDI Interface)	600-00329	\$ 1,850.00
SCSI Board	600-01020	Please call
DSP~LINK Prototype Module	600-00338	\$ 95.00
Dual-Processor Communications Module	600-00347	\$ 95.00
Linear Codec Module	600-00563	\$ 395.00

VME PRODUCTS

DSP56001 VME Board	600-00446	\$ 5,995.00
Program RAM Upgrade - 0 wait state (35ns)		
Each 32K x 24 increment	202-00259	Please call
Maximum upgrade is 64K x 24 with EPROMs removed		
Data RAM Upgrade - 0 wait state 935ns)	202-00105	Please call
32k x 24 in each of X and Y memory space	202-00105	Please call
Dual TMS320C30 VME Board	600-01002	Please call

SOFTWARE DEVELOPMENT TOOLS

TMS320C1x Software Development System	600-00392	\$ 995.00
TMS320E1x EPROM Programming Module	600-00400	\$ 395.00
TMS320C14 In-circuit Emulator (ICE)	600-00419	\$ 3,495.00
Texas Instruments TMS320C25		
Texas Instruments COFF Assembler/Linker	100-00225	\$ 500.00
Texas Instruments COFF Assembler/Linker and C Compiler	100-00117	\$ 2,500.00
LSI Assembler/Linker and C Compiler	100-00126	\$ 995.00
Motorola DSP56001		
Motorola Assembler, Linker/Librarian, and Simulator	100-00199	\$ 495.00
Motorola C Compiler	100-00180	\$ 709.00
Motorola DSP96002		
Motorola Assembler, Linker/Librarian, and Simulator	100-00545	\$ 495.00
Motorola C Compiler	100-00554	\$ 709.00
Intermetrics Assembler	100-00563	\$ 1,000.00
Intermetrics C Compiler	100-00572	\$ 2,425.00
AT&T DSP32C		
AT&T Assembler/Linker and Simulator	100-00306	\$ 500.00
AT&T Applications Library	100-00324	\$ 100.00
AT&T Assembler/Linker, Simulator, C Compiler, and Support Library	100-00315	\$ 1,500.00
Application Software		
DADiSP Data Analysis Software Version 1.05	100-00054	\$ 895.00
DADiSP Data Analysis Software Version 2.00	100-00397	\$ 1,695.00
DISPRO Digital Filter Design Software Version 1.8	100-00063	\$ 995.00
Software Integrated With SPECTRUM Hardware		
Speech Workstation (Requires TMS320C25-50 MHz Processor with 64K)	600-00932	\$ 4,715.00
Hypersignal Workstation	100-00243	\$ 989.00
Hypersignal-Plus	100-00441	\$ 489.00
Momentum Filter Design Software Version 1	100-00261	\$ 695.00
Momentum Filter Design Software Version 2	100-00270	\$ 1,095.00

ADVANCED INFORMATION PRODUCTS

Please call for Price and Availability.

DOCUMENTATION ONLY FOR MOST DSP BOARDS	\$ 35.00
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SPECTRUM's DSP BOARD INFORMATION CARD

Spectrum would like to provide you with advance information on all of our new products! In order to design products that meet your needs, please complete this questionnaire, fold it, tape it and mail it. We'll send you our "Einstein" Poster as a gift.

Name _____ Title _____

Company _____

Address _____

City _____ State _____ Zip Code _____

Country _____ Facsimile _____ Telephone _____

1. My company sells to the following industries:

_____ Telecommunications _____ Medical _____ Industrial/Control _____ Multi-Media
_____ Defense/Aerospace _____ Digital Audio _____ University _____ Other: _____

2. My DSP Application is:

_____ Digital Audio _____ Educational _____ Eval/Research _____ Image Processing
_____ Industrial Control _____ Medical _____ Radar/Sonar _____ Data Acquisition
_____ Test & Measurement _____ Satellite _____ Speech syn/recog _____ Telecommunications
_____ Intelligence/surveillance _____ Instrumentation _____ Robotics _____ Other _____

3. The estimated volume for my DSP application will be:

_____ Less than 100 units per year _____ 100 to 500 units per year _____ 501 to 1,000 units per year
_____ 1,001 to 10,000 units per year _____ 10,001 to 50,000 units per year _____ Over 50,000 units per year

4. I would ☐ would not ☐ consider an OEM DSP product.

5. When making a buying decision, the most important considerations are: (1 as highest, 10 as lowest)

	<u>Development Systems</u>	<u>OEM Purchases</u>
Price	_____	_____
Applications Engineering	_____	_____
Post-Sales Technical Support	_____	_____
Delivery Capability	_____	_____
Vendor Reputation	_____	_____
Software Development Tools	_____	_____
Product Flexibility	_____	_____
In-House Capabilities	_____	_____
Speed of Design	_____	_____
Speed of Product to Market	_____	_____

6. I am most interested in the following DSPs:

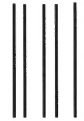
<u>DSP</u>	<u>Reason</u>	<u>DSP</u>	<u>Reason</u>
TI's TMS320C25	_____	TI's TMS320C50	_____
TI's TMS320C30	_____	Motorola's DSP56001	_____
Motorola's DSP56116	_____	Motorola's DSP96002	_____
AT&T's DSP32C	_____	AT&T's DSP16C	_____
Analog Devices' ADSP-2100	_____	Analog Devices' ADSP-2101	_____
NEC's UPD77230	_____	Zoran DSPs	_____
Other _____	_____		

7. I learn about new DSP products through:

_____ Trade Shows/Conferences _____ Advertising _____ Editorials _____ Colleagues
_____ Company Newsletters _____ Sales People _____ Seminars _____ DSP Manufactureres

8. SPECTRUM's next DSP product should be a:

RECEIVE A FREE EINSTEIN POSTER WHEN YOU RETURN THIS QUESTIONNAIRE!



NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

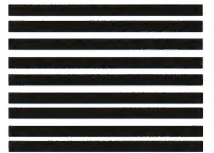
BUSINESS REPLY MAIL

FIRST CLASS MAIL PERMIT NO.206 BLAINE, WA

POSTAGE WILL BE PAID BY ADDRESSEE

SPECTRUM  SIGNAL PROCESSING INC

264 'H' STREET
P.O. BOX 8110-25
BLAINE, WA 98230



Warranty and Service Policies

This Guide is intended to communicate SPECTRUM's Warranty and Service Policies. If you want clarification or need help to deal with a situation not covered here, simply telephone the SPECTRUM office nearest you.

WARRANTY

All standard SPECTRUM hardware products are warranted against defective materials and workmanship for a period of one year from the date of invoice to the original purchaser. Any product that is found to be defective within the warranty period will, at the option of SPECTRUM, be repaired or replaced.

LIMITATIONS OF WARRANTY AND REMEDY

The Warranty set forth above does not extend to, and shall not apply to products which have been repaired or somehow altered by personnel other than SPECTRUM's (including removal of the serial number) unless the Customer has properly altered or repaired the products in accordance with procedures previously approved in writing by SPECTRUM; nor does the Warranty extend to products which have been subject to misuse, neglect, damage, radical environmental conditions or improper handling.

There are no implied warranties of merchantability or of fitness for a particular purpose given in connection with the sale of any SPECTRUM products. SPECTRUM assumes no liability for incidental, consequential or special damages of any kind arising out of the sale, installation or use of its products. SPECTRUM neither assumes nor authorizes the assumption of any other liability in connection with the sale, installation or use of its products. SPECTRUM assumes no liability whatsoever for inclusion of its products in critical medical systems. In no case will SPECTRUM's liability under this warranty or under any legal theory exceed the purchase price of this product.

EFFECTIVE PERIOD OF WARRANTY

All SPECTRUM hardware is warranted for a period of one year from date of invoice. Repaired or replacement components are warranted for a period of 30 days from date of repair (repaired or replaced component only).

RETURN PROCEDURES FOR WARRANTY WORK AND SERVICE REPAIRS

If a product should fail during the Warranty Period, it will be repaired or replaced free of charge. For "out of Warranty" repairs, the Customer will be invoiced for repair charges. Once the Customer determines that repair work is required (with the telephone assistance of SPECTRUM technical personnel, if required), the Customer is requested to:

1. Obtain a "Return Material Authorization" (RMA) number by calling 800-663-8986 (if calling in the USA) or (604) 438-7266 (if in Canada or overseas) and providing the Serial Number of the product.
2. Carefully package the product in the anti-static packaging in which the board was received (if available) and ship prepaid to SPECTRUM. Please show the RMA number and Serial Number on the outside of the package. It is important that the Customer provide a written description of the malfunction, along with return address and telephone number of a technical contact.

SERVICE AND REPAIR POLICY

For products under Warranty:

Upon completion of repair work, SPECTRUM will provide a statement of work done and will return the product via UPS Ground. For "Rush" returns, repaired items will be sent by the method specified by the Customer.

For products "out of Warranty":

All "out of Warranty" repairs will be invoiced at material replacement charges and technician's service time at US\$50.00 per hour. Shipping charges (both ways) are the responsibility of the Customer. We endeavour to turn around Customer repairs as rapidly as possible. If a "Rush" situation exists, please notify SPECTRUM when obtaining the RMA number and we will do our best to accommodate your needs.

SPECTRUM Signal Processing reserves the right to modify or discontinue any product at any time without notice.

MISSION STATEMENT

***SPECTRUM Signal Processing is committed
to helping customers develop better products by making
DSP technology more accessible.***

***We are a technology company that provides a "total
solution" from concept to completion.***

***We achieve our goals by understanding the needs of our
customers, developing quality products, and building strategic
relationships with key players in the DSP marketplace.***

For Engineering, Sales and Technical support, call:

In the Eastern US, 1-800-323-1842

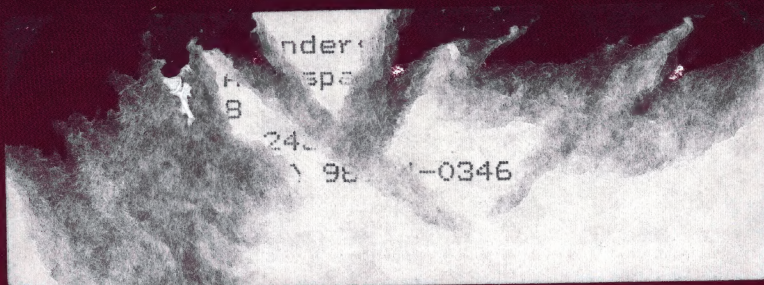
In the Western US, 1-800-663-8986

In Canada, (604) 438-7266

Spectrum Signal Processing Inc.
264 'H' Street, P.O. Box 8110-25, Blaine, WA 98230

Forwarding and return postage guaranteed.

BULK RATE
U.S. POSTAGE
PAID
Blaine, WA
Permit No. 106



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SIGNAL
PROCESSING INC.**

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605 - 01190

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